FINAL TECHNICAL DOCUMENTARY REPORT

HIGH-SPEED MICROPOWER
MICROELECTRONIC LOGIC CIRCUITS

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For the Period
18 May 1967— 18 June 1968
Contract No. NAS1-7106

Prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
LANGLEY RESEARCH CENTER
Hampton, Virginia

TEXAS INSTRUMENTS INCORPORATED
P.O. Box 5012
Dallas, Texas 75222

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FOREWORD

This program for the development of "High-Speed Micropower Microelectronic Logic Circuits" was carried out by Texas Instruments Incorporated in Dallas, Texas under Contract No. NAS1-7106 for NASA, Langley Research Center, Hampton, Virginia.

The work was done in the Semiconductor Research and Development Laboratory, Molecular Electronics Programs Branch (Dr. W. T. Matzen, Manager), and Micropower Section (Dr. D. J. Manus, Section Head).

This report was written by R. Stehlin, Project Engineer, with contributions by W. Cashion, Diffusion Engineer, and G. Threadgill, Engineering Assistant.

The work reported here represents an advancement in the state of the art in that complementary transistors in integrated-circuit form have been developed and used in low-power, low-voltage, high-speed logic circuits.

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ABSTRACT

This is the final technical documentary report on High-Speed
Micropower Microelectronic Logic Circuits, Contract No.
NAS1-7106, prepared for the National Aeronautics and Space
Administration, Langley Research Center, Hampton, Virginia. The
report describes the development of Complementary Transistor-
Transistor Logic (CT^2L) for use at high speeds (2 MHz), while
maintaining very low worst-case standby power (300 μW). Also
described is the development of three circuits and their fabrication
by the master bar approach. They are: 1) a single-6 input NAND
gate, 2) a dual-3 input NAND gate, and 3) a J-K Flip-Flop. Results
have shown that CT^2L logic can be used as a high-speed logic at
micropower levels. The circuits operate at a 200 μW level at 50 kHz
and have worst-case standby powers of less than 300 μW. Operating
frequencies of over 2.0 MHz have been obtained at these power
levels. The NAND gates exhibit a power-speed product of 14
picojoules and the Flip-Flops have power-speed product of 9
picojoules. Two methods of obtaining complementary transistors in
integrated form are described. Both the NPN and PNP devices have
excellent matched low-current characteristics. These devices have
application in the linear field as well as the digital field. Further
reduction in power and increase in operating frequency is predicted
for improved isolation techniques.

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SECTION I

INTRODUCTION

This final report on the development of "High-Speed Micropower Microelectronic Logic Circuits" documents the effort expended and performance achieved under contract NAS1-7106, for the period 1 May 1968 through 16 June 1968.

The program represents an extension of micropower research and development performed under contract NAS1-4350. In this contract, under the guidance of NASA, complementary logic was selected as the best approach to achieving low power and high performance. During the course of development, a new circuit approach to micropower logic envolved. Called complementary transistor-transistor-logic (CT^2L), it made possible an order of magnitude improvement in switching speeds at micropower levels.

The objective of this program was twofold—simplification of fabricating complementary (PNP and NPN) transistors on a single silicon bar, and fabrication of three types of circuits. These circuits were: 1) a 6-input NAND gate, 2) a dual 3-input NAND gate, and 3) a J-K Flip-Flop. The circuits had the design characteristics of: 1) "0" worst case standby power per gate (or flip-flop) of less than 300 μW, and 2) a maximum frequency of operation of greater than 2 MHz.

SECTION II

TECHNICAL DISCUSSION—DESIGN AND EVALUATION

A. HISTORY

The concept of using complementary (PNP and NPN) transistors in logic circuits was advanced by Baker,[1] for obtaining a maximum efficiency design. The features of a circuit that uses complementary transistors at the output are:

1) Drive capabilities are excellent since the load is driven by a low-impedance source in both directions

2) Essentially all the output current is available to drive the load

3) Both the high and low output voltages are clamped by the $V_{CE(sat)}$ of the transistors

4) Fast switching speeds are inherent at low power

5) There is low standby power; i.e., when there is NO LOAD, the power dissipated is that of the base resistors

6) The tolerance on all resistors may be large

7) Circuit operation is substantially independent of transistor parameters

8) Circuit stability is insensitive to supply voltages

9) Circuit operates with only one power supply.

This new approach to high-speed, micropower logic, developed during the performance of contract NAS1-4350,[2] combined the inherent low standby power of the complementary inverter with the high speed of T^2L-type input. This new logic (CT^2L) achieves faster switching speeds and repetition rates and shorter propagation delays at lower powers without sacrifice of other important characteristics such as noise margin and operation over a wide temperature range. This is achieved in a configuration which lends itself to fabrication in monolithic form.

B. COMPLEMENTARY SWITCH DESIGN

The basic complementary switch is inherently efficient. The input-output curve in Figure 1 describes the dc characteristics. Several important factors are noted in the following paragraphs.
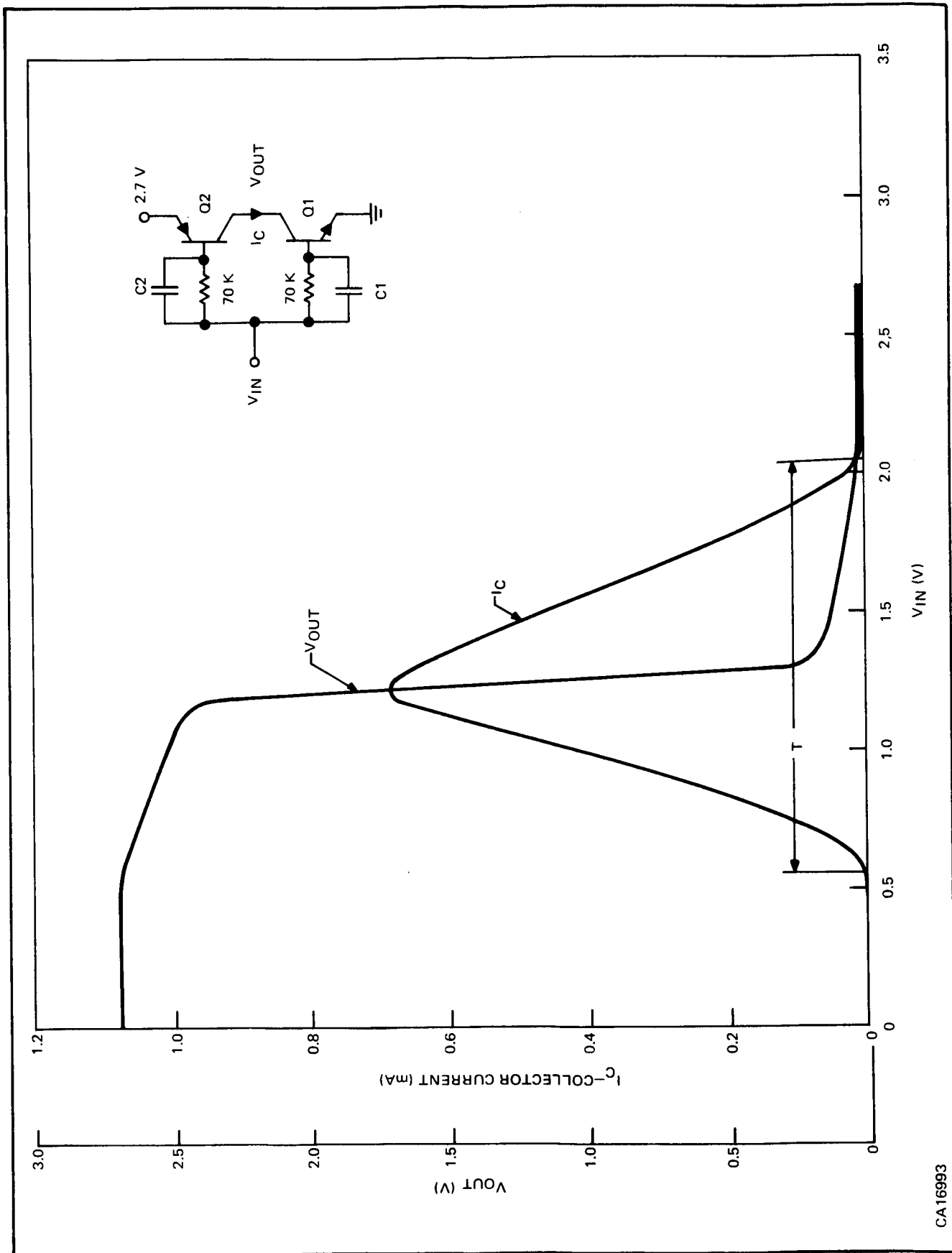
Figure 1. DC Switching Characteristics of Complementary Inverter

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1. Low Transistor Base Current

At either the "1" or "0" input, the only current drawn under NO-LOAD condition is the base current.

$$I_B = \left[\frac{V_{CC} - V_{CE(sat)} - V_{BE}}{R_B} \right] \tag{1}$$

This current can be made arbitrarily low, limited only the the low-current h_{FE} characteristics of the transistors.

2. High-Speed Switching Transistors—Low Power Dissipation

During transition times, collector current flows through both PNP and NPN transistors and is given by

$$I_C = \left[\frac{V_{IN} - V_{BEQ1}}{R_B} \right] h_{FEQ1}, \quad \text{for } V_{BE} \leqslant V_{IN} \leqslant \frac{V_{CC}}{2} \tag{2}$$

$$I_C = \left[\frac{V_{CC} - V_{BEQ2} - V_{IN}}{R_B} \right] h_{FEQ2}, \quad \text{for } \frac{V_{CC}}{2} \leqslant V_{IN} \leqslant V_{CC} - V_{BE} \tag{3}$$

For $h_{FEQ1} = h_{FEQ2}$, the maximum current occurs at $V_{IN} = (V_{CC})/2$

Therefore the PEAK current will be

$$I_{PEAK} = \left[\frac{V_{CC}/2 - V_{BE}}{R_B} \right] h_{FE} \tag{4}$$

In order to minimize power, the transition period T must be as short as possible. Bypass or "speed-up" capacitors C1 and C2 (Figure 1) must be used in parallel with the base resistors. The power dissipated by the charging and discharging of these capacitors becomes a significant portion of the total power at high frequency. When sufficiently large capacitors are used, the transition time is determined by the f_t of the transistors and parasitic capacitance.

3. Maximum Noise Immunity

The V_{IN} versus V_{OUT} curve shows that switching also occurs at $V_{IN} = (V_{CC})/2$, giving excellent noise immunity.

The factors which influence minimum standby power then become: 1) low current h_{FE}, and 2) resistor size. The factors that influence minimum power as a function of frequency are: 1) transistor h_{fe}, 2) f_t, and 3) parasitic capacitance.

C.   CT²L CIRCUIT ANALYSIS

1.   NAND Gate Analysis

a.   General

The NAND gate circuit used (Figure 2) is basically the same as that employed in NASA contract NAS1-4350. The major circuit design problem was to optimize the circuit for operation of 2 MHz while maintaining less than 300-μW power dissipation in the logic "0" worst-case standby condition.

The operation of the gate can be understood by referring to the schematic of the circuit in Figure 2.

The AND positive logic function is performed by the action of the multi-emitter transistor Q3. The NOT positive logic function is performed by the complementary output transistors Q1 and Q2. For the case in which any input is at a "0", base current flows through R1 from V_{CC} supplying base drive to Q3. This current turns Q3 on, supplying base current to Q1 through R2 and CR1. For the case of all inputs at a logic "1", all gating emitters are reverse-biased and base current is supplied to Q2 through Q4 and R4. The advantage of this circuit is that, in both cases, current is supplied through an active device providing symmetrical drive conditions to Q1 and Q2. This feature is the primary reason that fast switching speeds at low power levels are attainable.
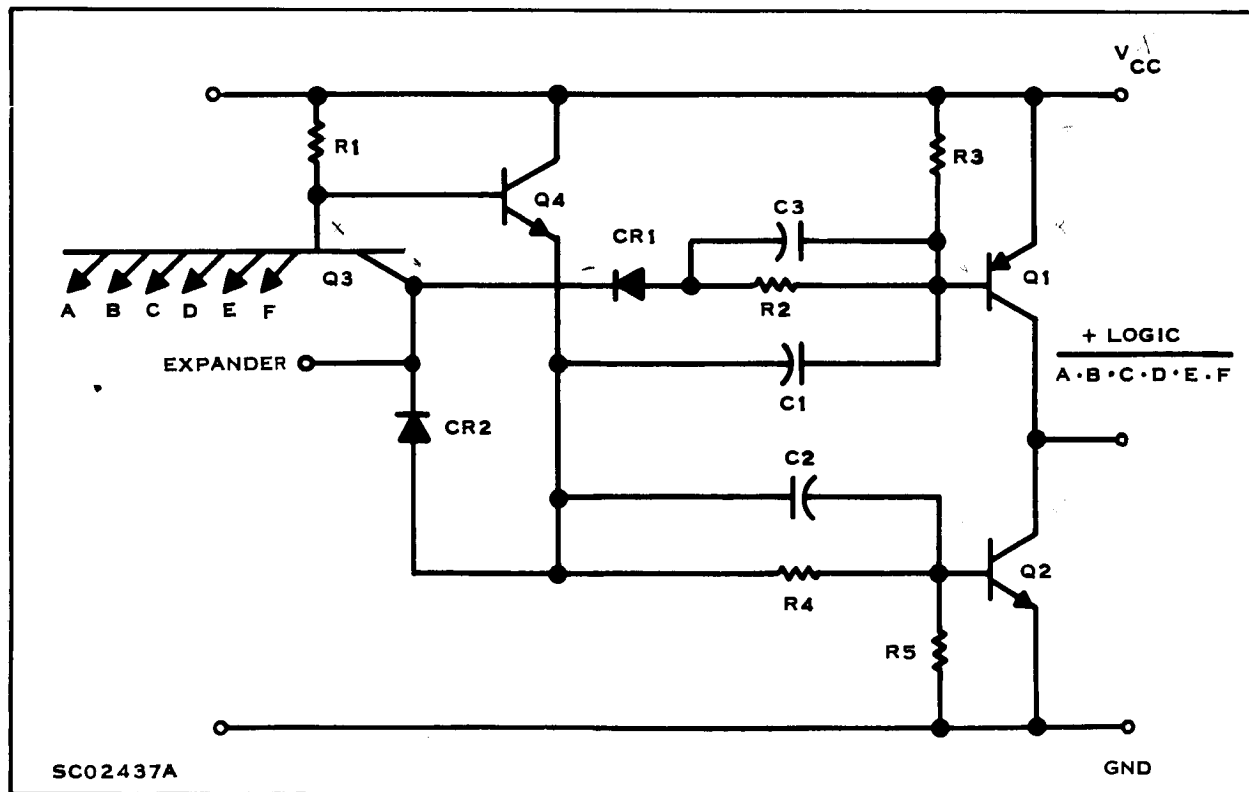

Figure 2.   CT²L NAND Gate

b. DC Analysis

Introduction. The worst-case dc conditions to be satisfied are:

Case 1) Q1 ON with "0" input at $-25°C$

Case 2) Q2 ON with "1" input at $-25°C$

Case 3) Q1 OFF with "1" input at $125°C$

Case 4) Q2 OFF with "0" input at $125°C$

The specification for loading is a fan-out of 5. The load current can be written as

$$I_{LOAD} = \left[I_{R1} + I_{R2} \right] \quad [\text{Fan-out}] \tag{5}$$

$$I_{LOAD} = \left\{ \left[\frac{V_{CC} (1 \pm X_V) - V_{CE(sat)} - V_{BE} \, N}{R1 (1 \mp X_R) M} \right] + \left[\frac{V_{CC} (1 \pm X_V) - 2V_{CE(sat)} - 2V_{BE} \, N}{R2 (1 \mp X_R) M} \right] \right\} \{5\} \tag{6}$$

where the following terminology and values are defined as:

$V_{CC} = 2.7$ V $\qquad\qquad$ X_V = tolerance of voltage = 5%

$V_{BE} = 0.7$ V $\qquad\qquad$ X_R = tolerance of resistor = 10%

$V_{CE(sat)} = 0.1$ V $\qquad\quad$ N = temperature coefficient of V_{BE}

Fan-out = 5 $\qquad\qquad\qquad$ M = temperature coefficient of diffused resistors

R1 = R2 = R4 = 40 kΩ $\qquad$ R3 = R5 = 80 kΩ

Using the appropriate values, the total dc load current can be written as:

$$I_{LOAD(max)} = \left\{ \left[\frac{2.735 - 0.7 \, N}{36 \cdot 10^3 \, M} \right] + \left[\frac{2.635 - 1.4 \, N}{36 \cdot 10^3 \, M} \right] \right\} \{5\} \tag{7}$$

At $-25°C$: N = 1.15, M = 0.9

$$I_{LOAD(max)} = 455 \, \mu A \tag{8}$$

Case 1) Q1 ON with "0" at -25°C.

$$h_{FEQ1(min)} = \frac{I_{LQ1(max)}}{I_{BQ1(min)}} \tag{9}$$

$$I_{BQ1} = I_{R2} - I_{R3} = \left[\frac{V_{CC}(1 \pm X_V) - 2V_{BE} \ N - 2V_{CE(sat)}}{R2 \ (1 \mp X_R) \ M}\right]$$

$$- \left[\frac{V_{BE} \ N}{R3 \ (1 \mp X_R) \ M}\right] \tag{10}$$

$$I_{BQ1(min)} = \left[\frac{2.365 - 1.4 \ N}{44 \cdot 10^3 \ M}\right] - \left[\frac{0.7 \ N}{72 \cdot 10^3 \ M}\right] \tag{11}$$

Under normal conditions, the dc drive requirement on the output transistor Q1 with a "0" input is, for all practical purposes, zero. Let us assume that the NAND gate will be required to drive a symmetrical load, i.e., $I_{LQ1(max)} = I_{LOAD(max)}$.

Therefore

$$h_{FEQ1(min)} = \frac{455 \ \mu A}{6.7 \ \mu A} = 68 \ at \ -25°C \tag{12}$$

Since $h_{FE(min)}$ will decrease from 25°C to -25°C, we determine the room temperature h_{FEQ1} as

$$h_{FEQ1(min)} = 68 \cdot \frac{1}{0.89} = 76 \ at \ 25°C \tag{13}$$

Case 2) Q_2 ON with "1" input at $-25°C$

$$h_{FEQ2(min)} = \frac{I_{LQ2(max)}}{I_{BQ2(min)}} \tag{14}$$

$$I_{BQ2} = I_{R4} - I_{R5} = \left[\frac{V_{CC}(1 \pm X_V) - I_{BQ4} \ R1 - 2V_{BE} \ N}{R4 \ (1 \mp X_R) \ M} \right]$$

$$- \left[\frac{V_{BE} \ N}{R5 \ (1 \mp X_R) \ M} \right] \tag{15}$$

Before proceeding, the term, "$I_{BQ4} \ R1$" must be solved. The input resistance of Q4 may be approximated by

$$R_{IN} \doteq h_{FE} \ R_L \tag{16}$$

$$\doteq h_{FE(min)} \ R4$$

Let h_{FE} at $-25°C = 100$; then

$$R_{IN} = 100 \cdot 40 \cdot 10^3 = 4.0 \cdot 10^6 \ \Omega \tag{17}$$

From which

$$I_{BQ4} = \frac{V_{CC}(1 \pm X_V) - 2V_{BE} \ N}{R1 + 4.0 \cdot 10^6} \tag{18}$$

$$= 0.32 \cdot 10^{-6} \ A$$

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and

$$I_{BQ4} \ R1 \ = \ 0.32 \ \cdot \ 10^{-6} \ \cdot \ 4.0 \ \cdot \ 10^4 \qquad (19)$$

$$= \ 0.013 \ V$$

and

$$I_{BQ2(min)} \ = \ \left(\frac{2.54 \ - \ 1.4 \ N}{44 \ \cdot \ 10^3 \ M} \right) - \left(\frac{0.7 \ N}{72 \ \cdot \ 10^3 \ M} \right) \qquad (20)$$

Let $\quad I_{LQ2(max)} \ = \ I_{LOAD(max)} \ = \ 455 \ \mu A$

then

$$h_{FEQ2(min)} \ = \ \frac{455 \ \mu A}{11.1 \ \mu A} \ = \ 41 \ \text{at} -25°C \qquad (21)$$

Taking into account the h_{FE} variation with temperature

$$h_{FEQ2(min)} \ = \ 41 \ \cdot \ \frac{1}{0.72} \ = \ 57 \ \text{at } 25°C \qquad (22)$$

Case 3) Q1 OFF with "1" input at 125°C. For all inputs at "1", Q3 is off. When Q3 is off, Q1 is held off by R3 to V_{CC}. If the inputs "1" fall low enough to cause Q3 to conduct, Q1 is still held off by the shift of CR1 and the dividing action of R2 and R3.

Case 4) Q2 OFF with "0" input at 125°C. For the case with one or more inputs at "0", Q3 conducts and Q2 is then held off by R5 to ground. If the input begins to rise, Q2 is held off by the shift of CR2 and the dividing action of R4 and R5.

c. **Standby Power Calculation**

Case 1) Clock at "1".

$$P_{dc1} = V_{CC} I_{CC}$$

$$= V_{CC} (1 \pm X_V) \cdot \left[\frac{V_{CC}(1 \pm X_V) - 2V_{BE} N - I_{BQ4} R1}{R4 (1 \pm X_R) M} \right] \tag{23}$$

The worst-case power considerations are at 25°C for this TCR; therefore

$$M = N = 1$$

thus

$$P_{dc1} = 2.835 \left[\frac{2.835 - 1.4 - 0.013}{36 \cdot 10^3} \right] \tag{24}$$

$$= 112 \ \mu W$$

2) Case 2) Clock at "0"

$$P_{dc0} = V_{CC} I_{CC}$$

$$= V_{CC} (1 \pm X_V) \left\{ \left[\frac{V_{CC} (1 \pm X_V) - V_{CE(sat)} - V_{BE} N}{R1 (1 \pm X_R) M} \right] + \right.$$

$$\left. \left[\frac{V_{CC} (1 \pm X_V) - 2V_{CE(sat)} - 2V_{BE} N}{R2 (1 \mp X_R) M} \right] \right\} \tag{25}$$

$$= 2.835 \left[\left(\frac{2.835 - 0.1 - 0.7}{36 \cdot 10^3} \right) + \left(\frac{2.835 - 0.2 - 1.4}{36 \cdot 10^3} \right) \right]$$

$$= 254 \ \mu W \tag{26}$$

To this must be added the additional power drain for the worst-case condition of one emitter to ground and the remaining input emitters to V_{CC}.

For the 3 input NAND gate:

$$P_{\beta I} = V_{CC} \ (2\beta_I \ I_B)$$

$$= V_{CC} \ (1 \pm X_V) \ \left[2 \cdot \beta_I \cdot \left(\frac{V_{CC} \ (1 \pm X_V) - N \ V_{BE} - V_{CE(sat)}}{R1 \ (1 \pm X_R) \ M} \right) \right]$$

$$= 2.835 \ \left[2 \cdot 0.1 \left(\frac{2.835 \ - \ 0.7 \ - \ 0.1}{36 \ \cdot \ 10^3} \right) \right] \tag{27}$$

$$= 32.2 \ \mu W \tag{28}$$

therefore

$$P_{dc0(Total)} = 254 + 32.2 = 286.2 \ \mu W \tag{29}$$

The average standby power is

$$P_{(avg)} = \frac{P_{dc0} + P_{dc1}}{2} = \frac{286.2 + 112}{2} = 200 \ \mu W \tag{30}$$

d.   Transition Analysis

  Case 1) Transition of input from "1" to "0". As the driving transitor saturates and the input of Q3 goes from a logic "1" to a logic "0", the base current for Q1 can be written as

$$i_b = \left[\frac{V_{CC} \ - \ 2V_{BE} \ - \ 2V_{CE(sat)}}{R_{(sat)Q2} \ + \ R_{(sat)Q3}} \right] \exp \ \left[-t/ \left(R_{(sat)Q2} + R_{(sat)Q3} \right) C3 \right] \tag{31}$$

Inserting the proper parameter values yields a time constant of ~ 20 ns. Rise times in this range have been measured.

Case 2) Transition of inputs from "0" to "1". As the emitter of Q3 rises from the "0" state to the "1" state, Q3 remains in an "on" condition until $V_{in} \geqslant 1$ V. At this point Q4 is turned "on" and provides base drive through C1 and C2. The delay time is determined by the effective capacitance at the base of Q3 in conjunction with R1.

This effective capacitance is composed of the following components:

a)   The emitter-base capacitance of all inputs.

b)   The collector-to-substrate capacitance of Q3.

c)   Lead to substrate capacitance.

d)   Junction capacitance of CR1 and CR2.

e)   C1 and C2 reflected back through Q4.

f)   Distributed capacitance of R1.

Of the above, the second component is normally of the largest magnitude. A reduction of this component through improved isolation techniques will greatly improve the performance of the CT^2L NAND gate.

e.   Breadboard Results

The breadboard was built to simulate the actual integrated circuit. The resistors and capacitors were diffused components in TO-5 cans and the active devices were basically the same as those devices which were to be built in integrated form under this contract.

The breadboard power-versus-frequency results are shown in Figure 3. The plot of propogation delay versus power, shown in Figure 4, was attained by varying V_{CC} from 2.0 V to 6.0 V. The voltage transfer curves are plotted in Figure 5. Later sections of this report show that the actual integrated circuit performance is very similar to the breadboarded circuit.

The complementary inverter section of the CT^2L NAND gate is a relatively high-speed and low-power device. The limiting performance factor is the turn-off time of the multi-emitter AND gate section. The original circuit was breadboarded with discrete passive devices (carbon resistor, mylar capacitor) and with a minimum of stray capacitance. The complementary transistors were the same as previously used, but the multi-emitter transistor Q3 was replaced by the same type transistor as the output NPN transistor. The resulting power-speed curve is shown in Figure 6. This plot illustrates the increased performance obtained for the case of reduced stray capacitance and a higher f_t transistor on the input.
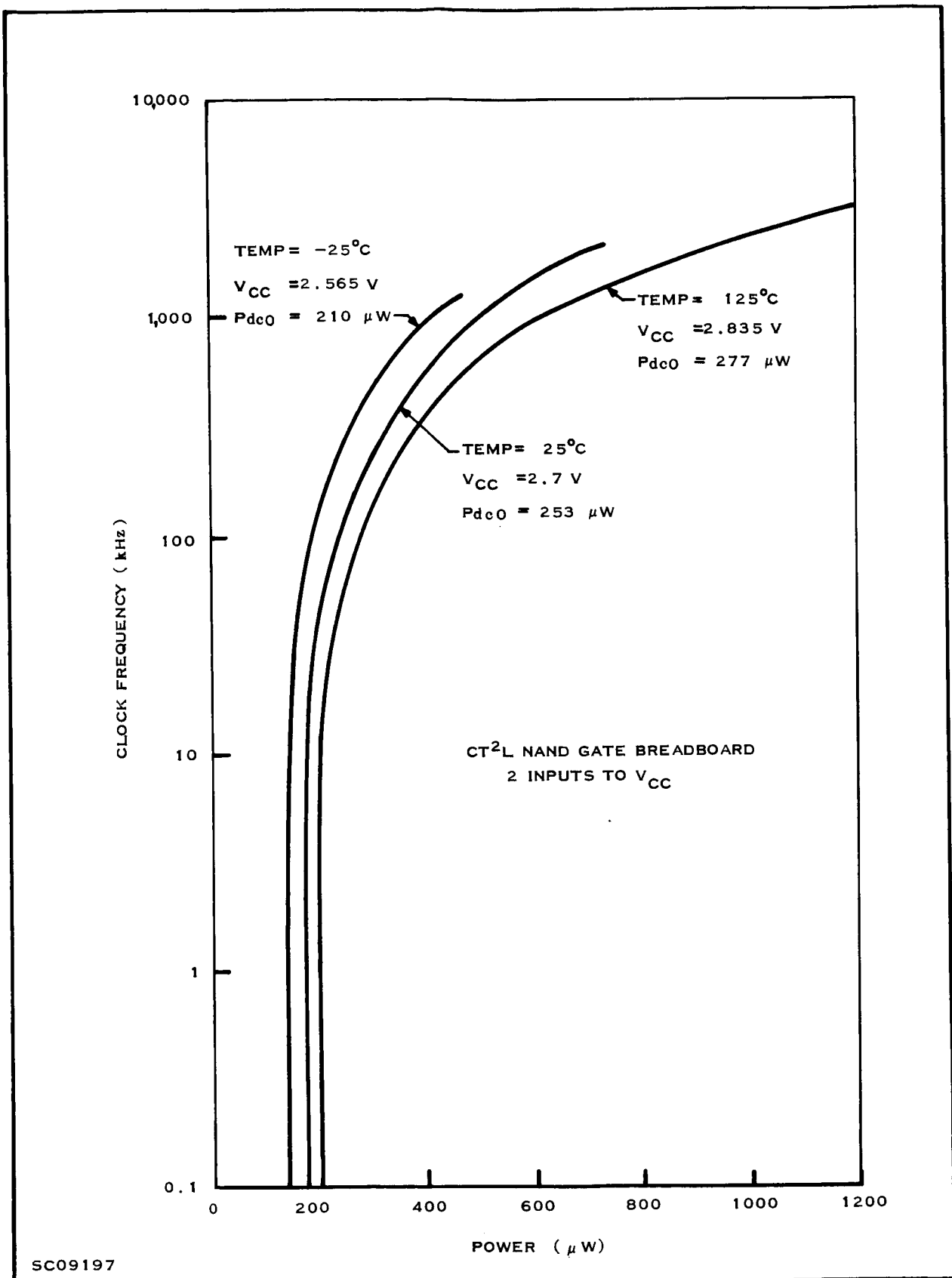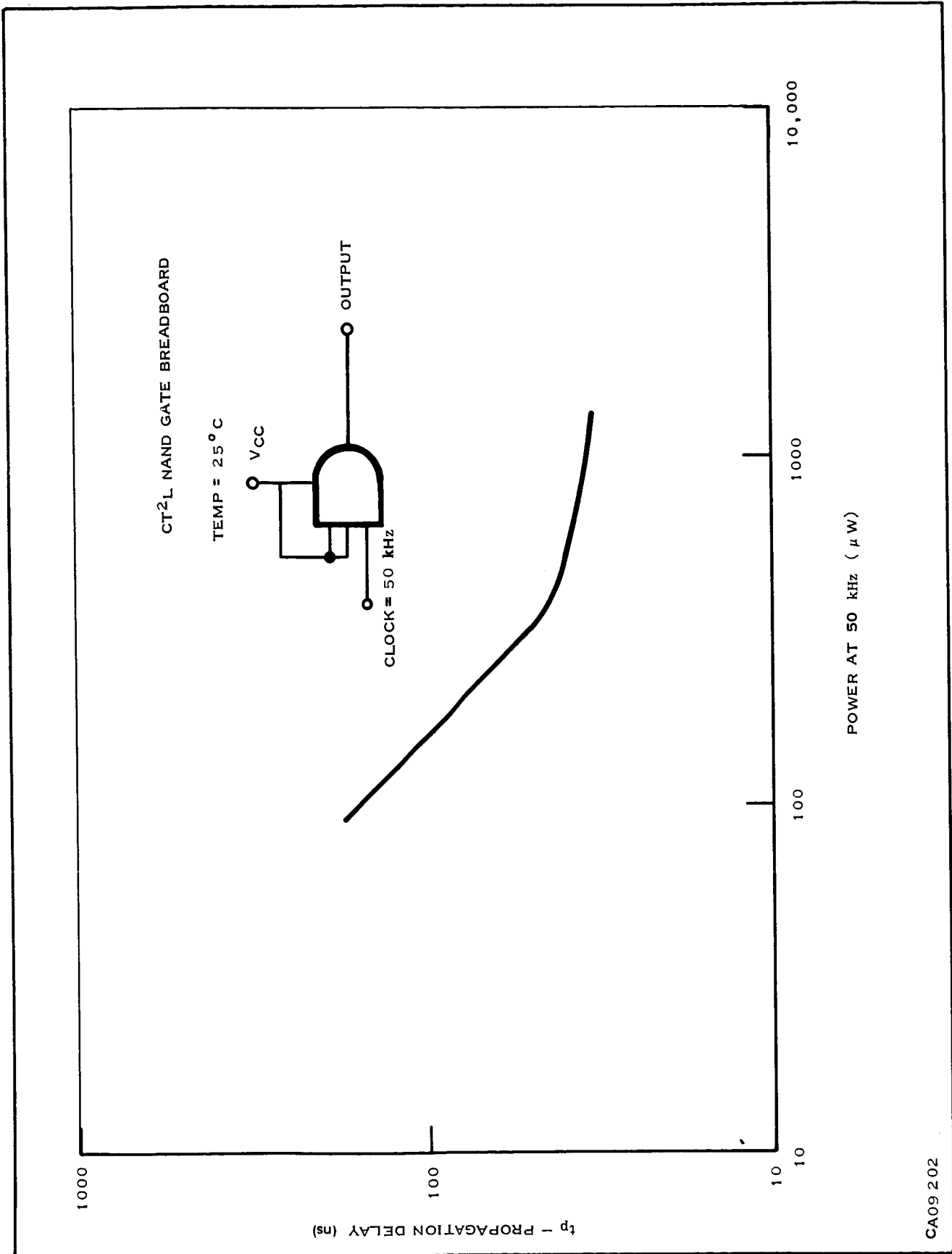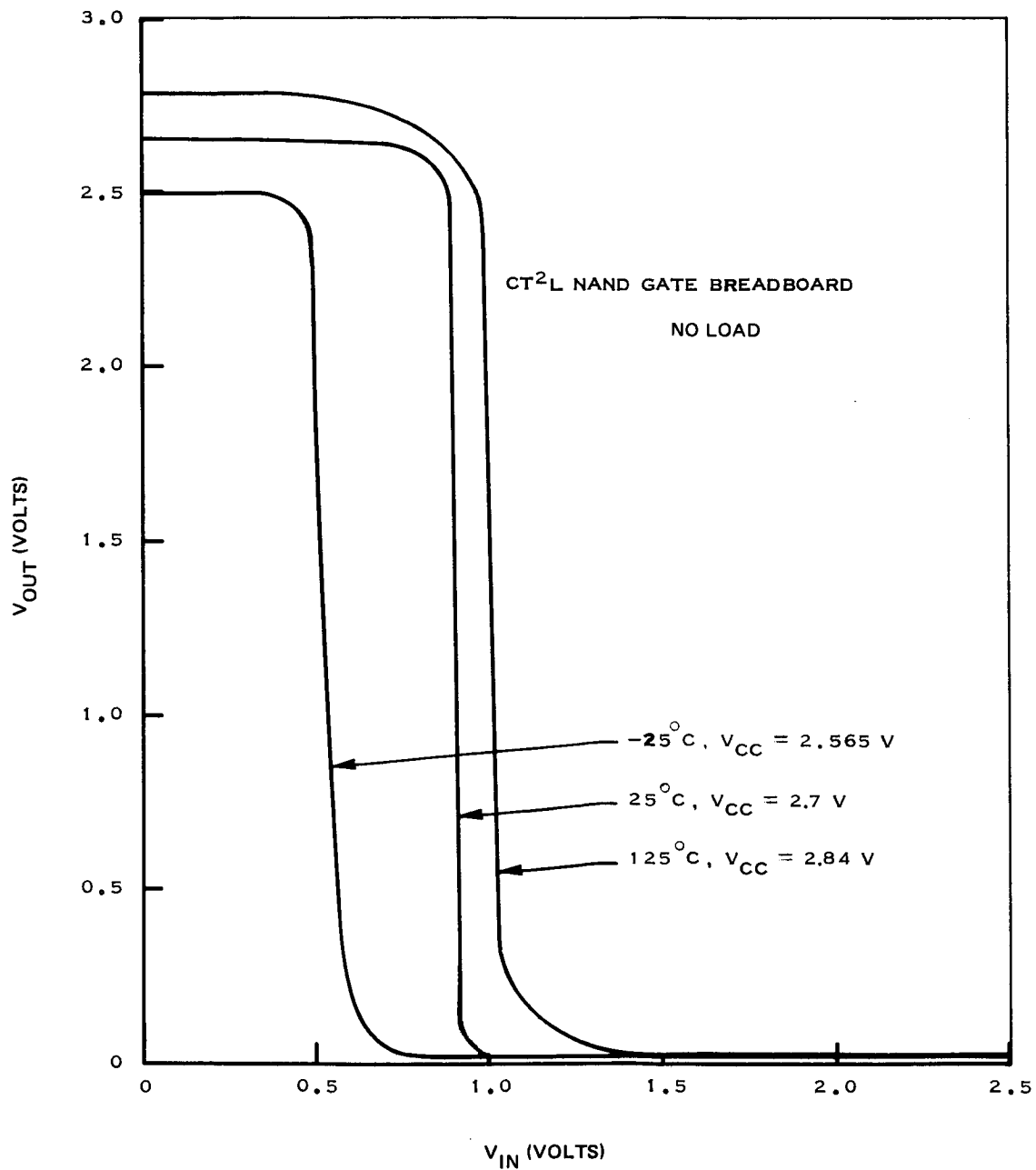
Figure 3. Power versus Frequency

Figure 4. Power–Speed Plot
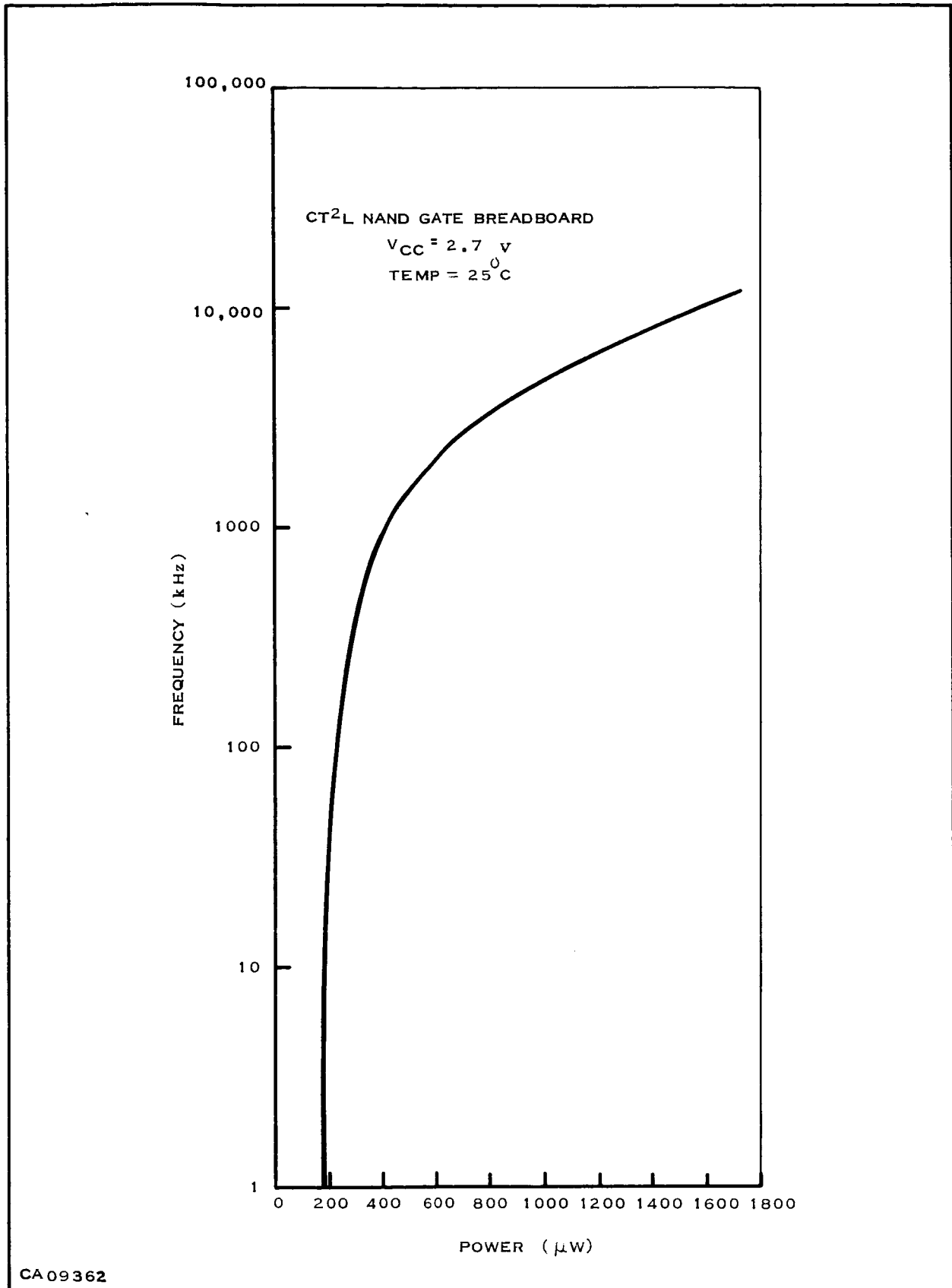
Figure 5. V_{IN} versus V_{OUT} Characteristics

Figure 6. Power versus Frequency (Using Discrete Devices)

2. **Flip-Flop Analysis**

a. General

The J-K Flip-Flop circuit used (Figure 7) is basically the same as that employed in NASA contract NAS1-4350. The major circuit design problem was to optimize the circuit for operation at 2-MHz clock frequency while maintaining less than 300-μW, power dissipation in the logic "0" worst-case standby condition.

The operation of the J-K Flip-Flop can be described by referring to the schematic of the circuit in Figure 7.

The basic bistable element is composed of two pairs of complementary transistors—Q1 and Q3; Q2 and Q4. In the stable state one, Q1 and Q4 are conducting while Q2 and Q3 are turned off. For stable state two, Q2 and Q3 are conducting while Q1 and Q4 are off. For stable state one, base current is supplied to Q4 through the resistor R3 and Q1 through resistor R2. For stable state two, base current is supplied to Q3 through R4 and to Q2 through R1.

The trigger (transistion action) is now considered. For this description, consider the circuit as a counter. (J-K inputs floating or to V_{CC}).

Assume the bistable element is in stable state one. In this state, trigger capacitor C1 has very nearly zero volts across it and is at a potential near V_{CC}. Also note that Q is at V_{CC} and consequently the top of R7 is at V_{CC}, charging C5 to $V_{CC} - V_{BE}$. This charge on C5 will deliver base current to Q7 during the transition. Note also that Q is at ground thereby inhibiting the J gate and holding the voltage on C6 to near 0 potential. The following sequence of regeneration occurs during the negative going transition of the clock.

1) As the clock input goes down, the emitter-base junction of Q7 is forward biased turning it on. This places the junction of R5 and C1 near ground potential.

2) Base current flows through Q2, C1 and Q7 turning on Q2.

3) The collector of Q2 rises to V_{CC} coupling a regenerative pulse through R4 and C4 to Q3 and through R2, R6 and C2 to Q1, turning off Q1.

4) With Q3 on and Q1 off, Q goes to zero volts, coupling regenerative pulses to Q4 through R3 and C3, turning Q4 off and through R1, R5 and C1 to Q2 holding Q2 on.

5) Regeneration is now complete and the circuit is in stable state two.

During the time when the clock is at zero volts, the J-K inputs are held at "0" level, thereby holding Q7 and Q8 off. Resistors R9 and R10 introduce a slight time delay, allowing the charge on C5 to discharge primarily through Q7 during the negative transition.

Continuing the sequence, when the clock input goes positive, a positive-going pulse is coupled through C10 to the base of Q10, turning Q10 on and allowing a rapid charge of C6. The bistable element is now set to start another cycle.

Q^n	J^n	K^n	Q^{n+1}
0	0	0	Q^n
0	0	1	0
0	1	0	1
0	1	1	$\bar{Q}^n$
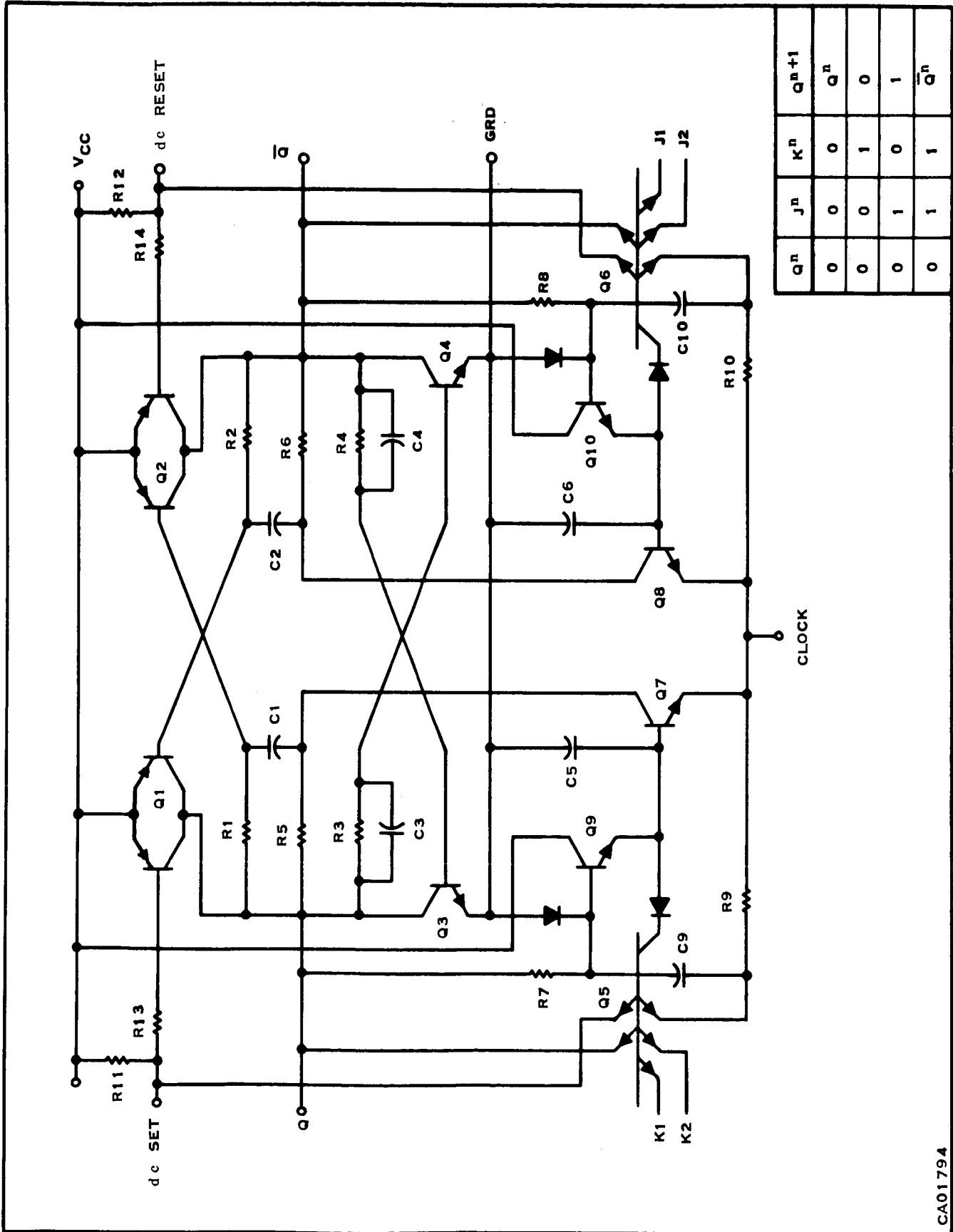
Figure 7. CT^2L Flip-Flop

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Straightforward ac and dc set and reset functions are provided which turn on Q1 or Q2 with a negative-going pulse at any of the above inputs.

b. DC Analysis

Assume that the worst-case loading is at $-25°C$ for a fan-out of five NAND gates. From calculations performed, we know that a fan-out of five flip-flops requires considerably less power than the five NAND gates. We also note from Figure 7 that the h_{FE} equation for Q1, Q2, Q3, and Q4 is the same.

$$h_{FE(min)} = \frac{I_{LOAD(max)}}{I_{B(min)}} \tag{32}$$

From Equation (8), the maximum load current $I_{LOAD(max)} = 455 \ \mu A$

$$I_{B(min)} = \frac{V_{CC} \ (1 \pm X_V) - V_{BE} \ N - V_{CE(sat)}}{R_B \ (1 \pm X_R) \ M} \tag{33}$$

where the same terminology as before holds and $R_B = 90 \ k\Omega$.

$$I_{B(min)} = \frac{2.46 - 0.7 \ N}{99 \cdot 10^3 \ M}$$

At $-25°C$

$$h_{FE(min)} = \frac{455}{18.5} = 24.6 \tag{34}$$

and at $25°C$

$$h_{FE(PNP)} = 24.6 \cdot \frac{1}{0.89} = 27.9 \tag{35}$$

$$h_{FE(NPN)} = 24.6 \cdot \frac{1}{0.72} = 34.6 \tag{36}$$

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c.   Standby Power Calculation

Case 1) Clock at "1".

$$P_{dc1} = V_{CC} I_{CC}$$

$$= V_{CC} (1 \pm X_V) \cdot 2 \left[\frac{V_{CC} (1 \pm X_V) - N V_{BE} - V_{CE(sat)}}{R_B (1 \mp X_R) M} \right] \quad (37)$$

$$P_{dc1} = 5.67 \left[\frac{2.735 - 0.7 \, N}{81 \cdot 10^3 \, M} \right]$$

Due to the temperature coefficient of the diffused resistors, the theoretical worst-case occurs at approximately 25°C (n=M=1). This does not include increased leakage at higher temperatures.

$$P_{dc1} = 143 \; \mu W \quad (38)$$

To this value must be added the power dissipation $P_{\beta I}$ due to the effect of emitter-to-emitter beta worst-case for the multi-emitter transistors Q5 and Q6. This power is given by

$$P_{\beta I} = V_{CC} (4\beta_I I_B)$$

$$= V_{CC} (1 \pm X_V) \cdot \left\{ \frac{4\beta_I \left[V_{CC} (1 \pm X_V) - N V_{BE} - 2V_{CE(sat)} \right]}{R_B (1 \mp X_R) M} \right\} \quad (39)$$

$$= 272 \; \beta_I \; \mu W \quad (40)$$

where β_I is the emitter-to-emitter current gain. From data taken on multi-emitter transistors with an external base resistor of 3 kΩ the worst-case value of β_I is expected to be 0.1. Therefore, $P_{\beta I} = 27.2$ μW. Total standby power in the "1" state is then the sum of P_{dc1} and $P_{\beta I}$, or 170.2 μW.

Case 2) Clock at "0".

$$P_{dc0} = P_{dc1} + V_{CC} (1 \pm X_V) \left[\frac{V_{CC} (1 \pm X_V) - 2V_{CE(sat)} - V_{BE} N}{R_{7-8} (1 \mp X_R) M} \right] \quad (41)$$

$$= 170.2 + 2.835 \left[\frac{2.635 - 0.7 N}{(81 \cdot 10^3) M} \right]$$

At 25°C, N = M = 1 so that

$$P_{dc0} = 170.2 + 67.7 = 237.9 \ \mu W \quad (42)$$

Average standby power $P_{(avg)}$ is given by

$$P_{(avg)} = \frac{P_{dc1} + P_{dc0}}{2} = \frac{170.2 + 237.9}{2} = 204.1 \ \mu W \quad (43)$$

d.   Breadboard Results

The Flip-Flop breadboard was constructed in a manner similar to the NAND gate construction. The breadboard results of Figure 8 indicate that there would be difficulty in obtaining 2 MHz if less than 300 μW standby were to be maintained. This is basically because we are operating one and one-half NAND gates at the same power level as one of the single-6 gates. By decreasing the gating transistor's base resistor, R_{7-8}, to 40 kΩ, the frequency can be obtained but at a sacrifice in standby power. A plot of power versus frequency for this condition is shown in Figure 9.

D.   DIFFUSION TECHNOLOGY

1.   Introduction

Since the completion of NASA Contract NAS1-4350, complementary transistor development has continued at Texas Instruments. The present process used to fabricate complementary transistors uses a buried-layer material. The buried-layer approach has an advantage over the previous methods of fabricating complementary transistors, in allowing for a reduction in the number of diffusion and photolithographic processing steps. This process will be designated "Schedule A" in this report.
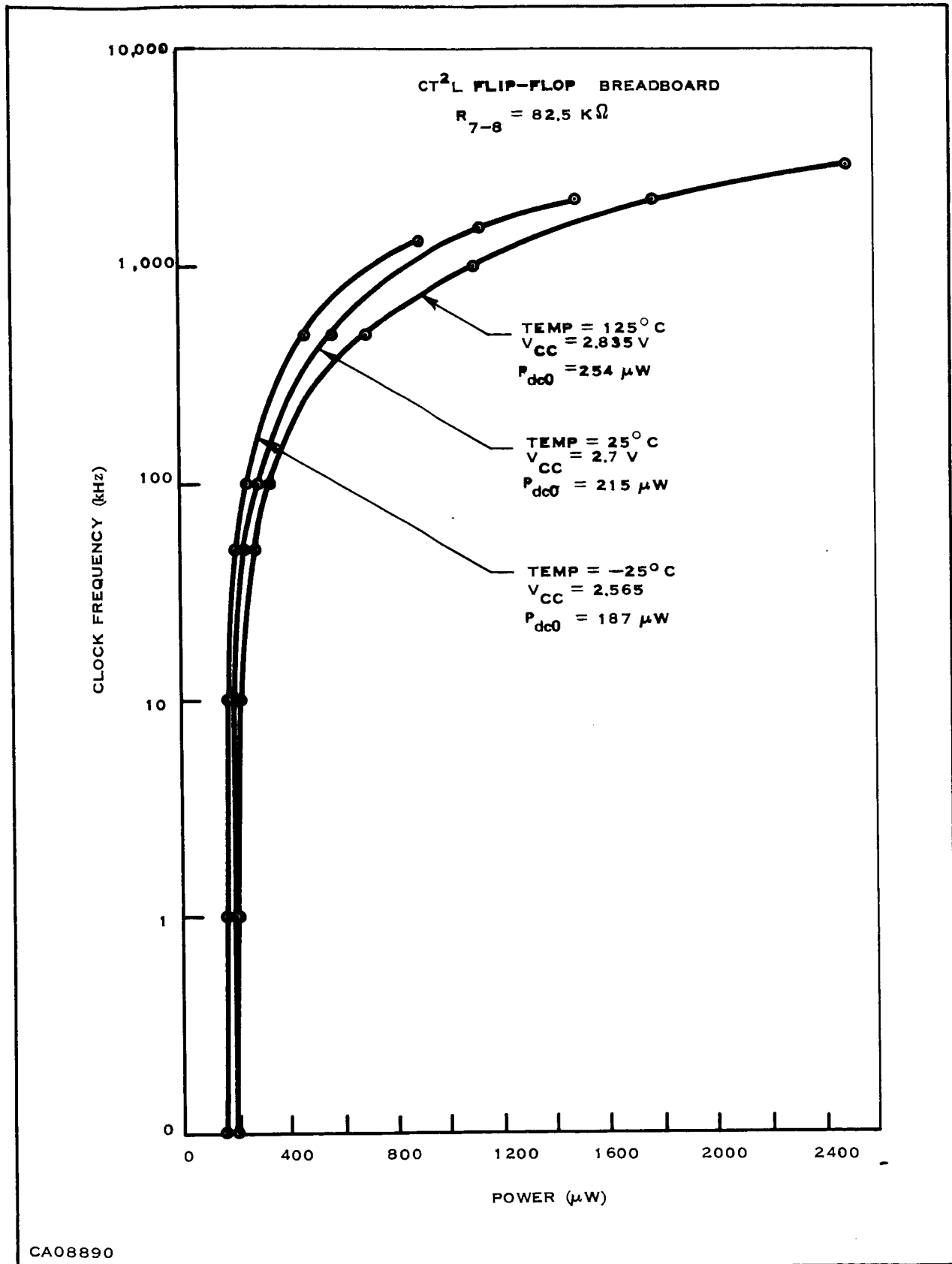
Figure 8.   Power versus Frequency, R_{7-8} = 82.5 kΩ
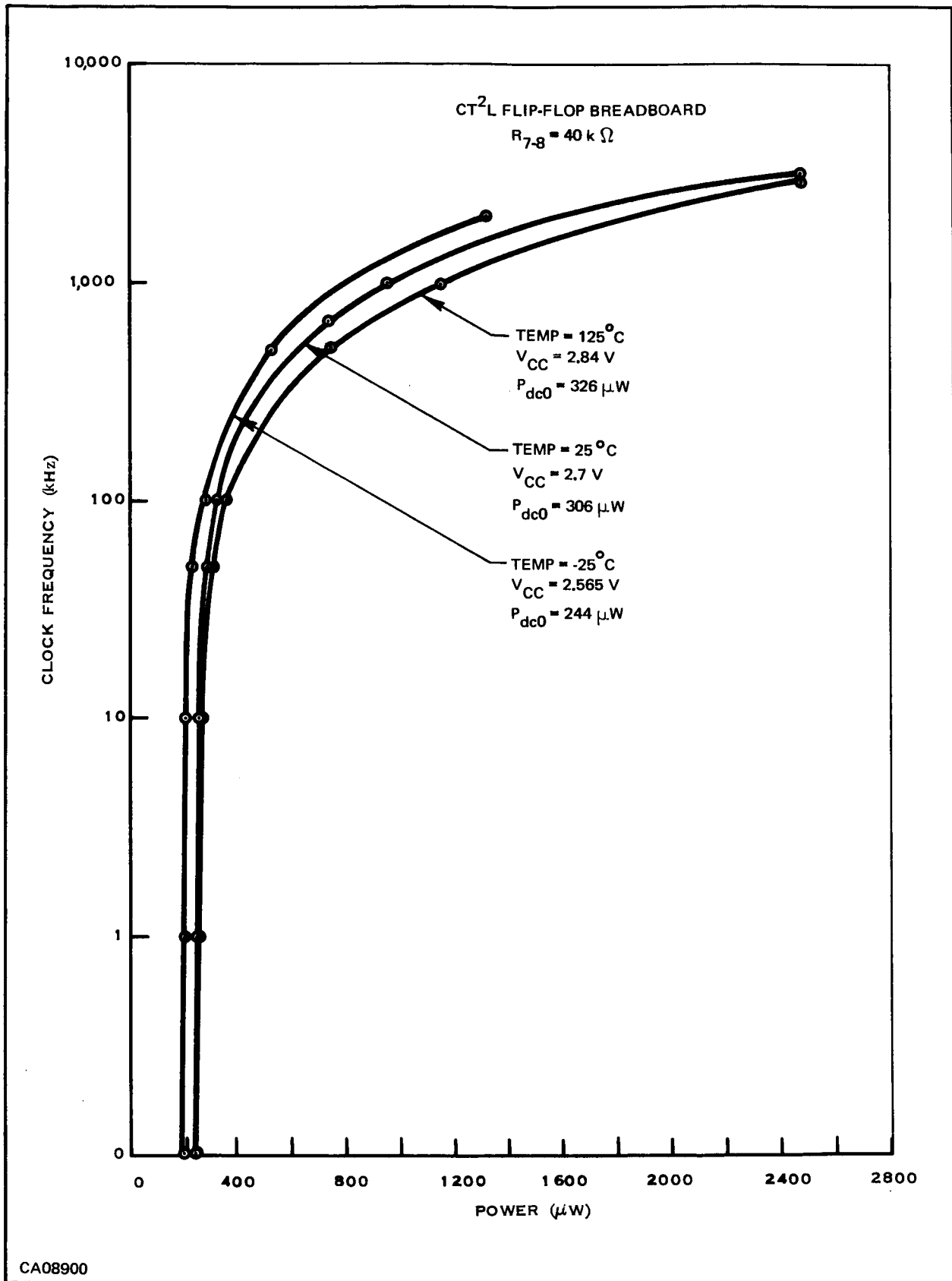
Figure 9.   Power versus Frequency, R_{7-8} = 40 kΩ

The goal of any process is to achieve the desired results with number of process steps. For best performance from the NPN and PNP transistors, independent diffusions should be used for each transistor. With these goals the minimum number of process steps (actual diffusions) would be three for PNP (triple-diffused) and two for the NPN (epitaxial collector). The above process has achieved the minimum processing steps and yields truly complementary transistors.

To eliminate some of the problems encountered in fabrication of Schedule A material, a new approach has been developed that uses a double buried layer. The new approach was developed to maintain a more consistent PNP base diffusion. This double buried-layer process will be designated "Schedule B" in this report. A further discussion of both processes will follow.

2. Buried-Layer Approach—Schedule A Process

The Schedule A approach for fabrication of complementary transistors is presented in Figure 10. The novelty of this process is in its use of the "buried layer" as a diffusion stop rather than its more conventional function of reducing collector series resistance. This allows for the formation of the PNP collector and the P-N junction isolation with the same diffusion. Impurity profiles for the NPN and PNP transistors of this structure are presented in Figs. 11 and 12.

Complementary transistors fabricated with this process exhibit excellent characteristics over a wide range of operating currents. Figure 13 shows the curve tracer results of a typical complementary pair of transistors using Schedule A. Some characteristic data on a typical unit are given in Figure 14 (h_{FE} versus I_E) and in Figure 15 (f_t versus I_E).

3. The Double-Buried Layer Approach—Schedule B Process

It should be made clear that the effort to develop a new process is not due to the quality of the transistor fabricated with the Schedule A approach. There have been at times noticeable inconsistancies with the fabrication of the PNP device in obtaining a uniform distribution of h_{FE}. The purpose of Schedule B was to match the performance of Schedule A devices while obtaining a more uniform distribution of current gain.

The background concentration (epitaxial layer) of Schedule A material is determined by the R_{sat} limit on the NPN transistor. The relatively high concentration of the epitaxial layer (0.2 Ω-cm) causes less than an order of magnitude difference between the collector and base region of the PNP transistor. Non-uniformity of the base region concentration has been a noticeable problem in fabrication of the PNP transistor.

The epitaxial thickness is dictated by the R_{sat} limit of the PNP transistor. An epitaxial layer of 10 μm is needed to assure obtaining a PNP collector junction of 8.5 μm. This relatively thick epitaxial layer renders useless the "buried-layer" region under the NPN transistor.

To eliminate some of the problems of the previous structure, a new approach has been developed which uses a double "buried-layer" material. The starting material is a standard "buried-layer" slice before the epitaxial layer has been grown. A standard P^+-type (boron)

(a) STARTING MATERIAL

(b) PNP COLLECTOR P-ISOLATION

$N_S = 1.5 \times 10^{18}$
$X_J = 8.5~\mu m$

(c) PNP BASE

$N_S = 1.5 \times 10^{19}$
$X_J = 1.6~\mu m$

(d) NPN BASE

$N_S = 5 \times 10^{18}$
$X_J = 0.96~\mu m$

(e) PNP EMITTER

$N_S = 5 \times 10^{20}$
$X_J = 1.1~\mu m$

(f) NPN EMITTER PNP-BASE CONTACT

$N_S = 8 \times 10^{20}$
$X_J = 0.7~\mu m$

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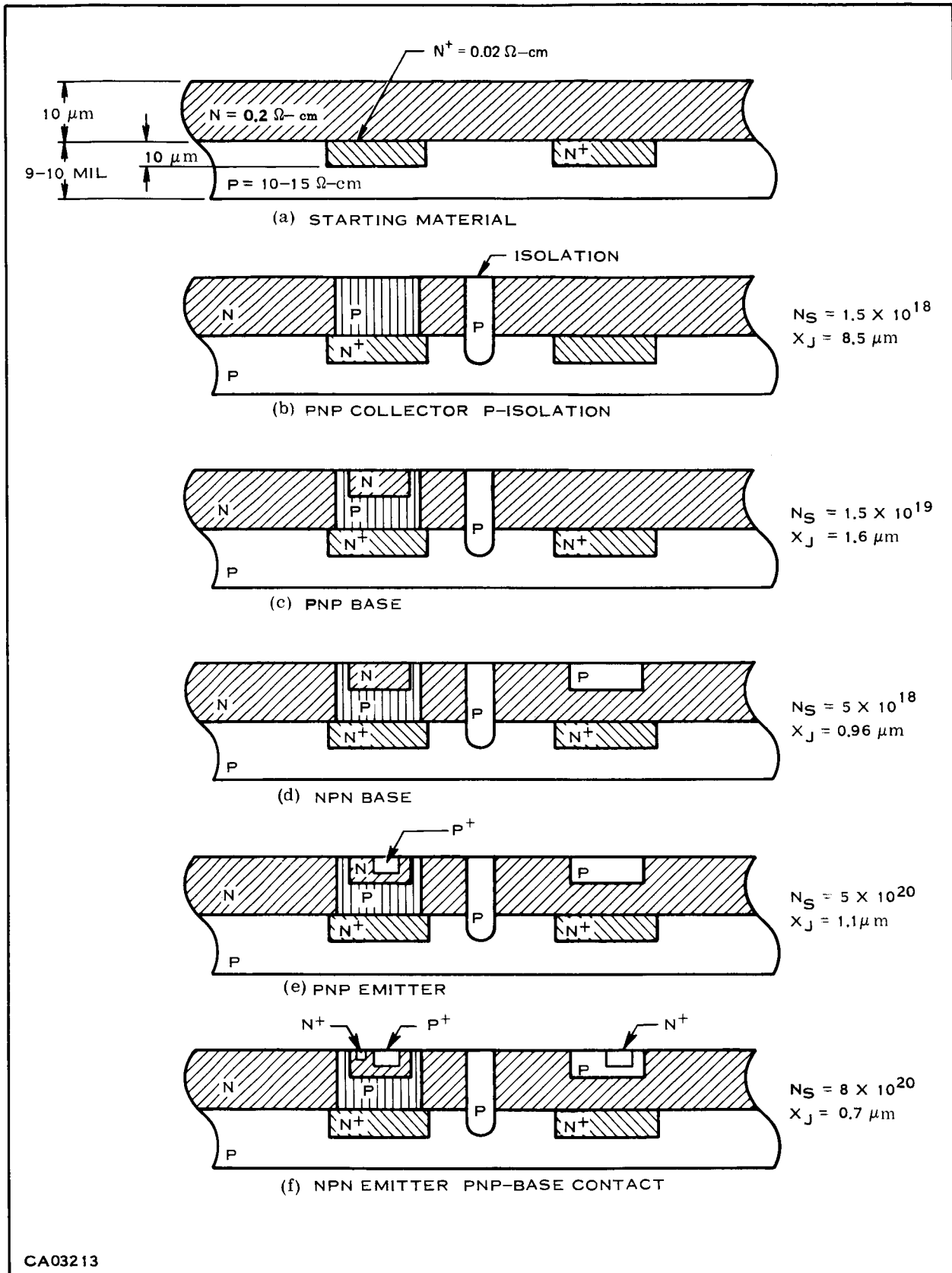
Figure 10.   All-Diffused PN Junction Isolated Buried-Layer–Schedule A Process
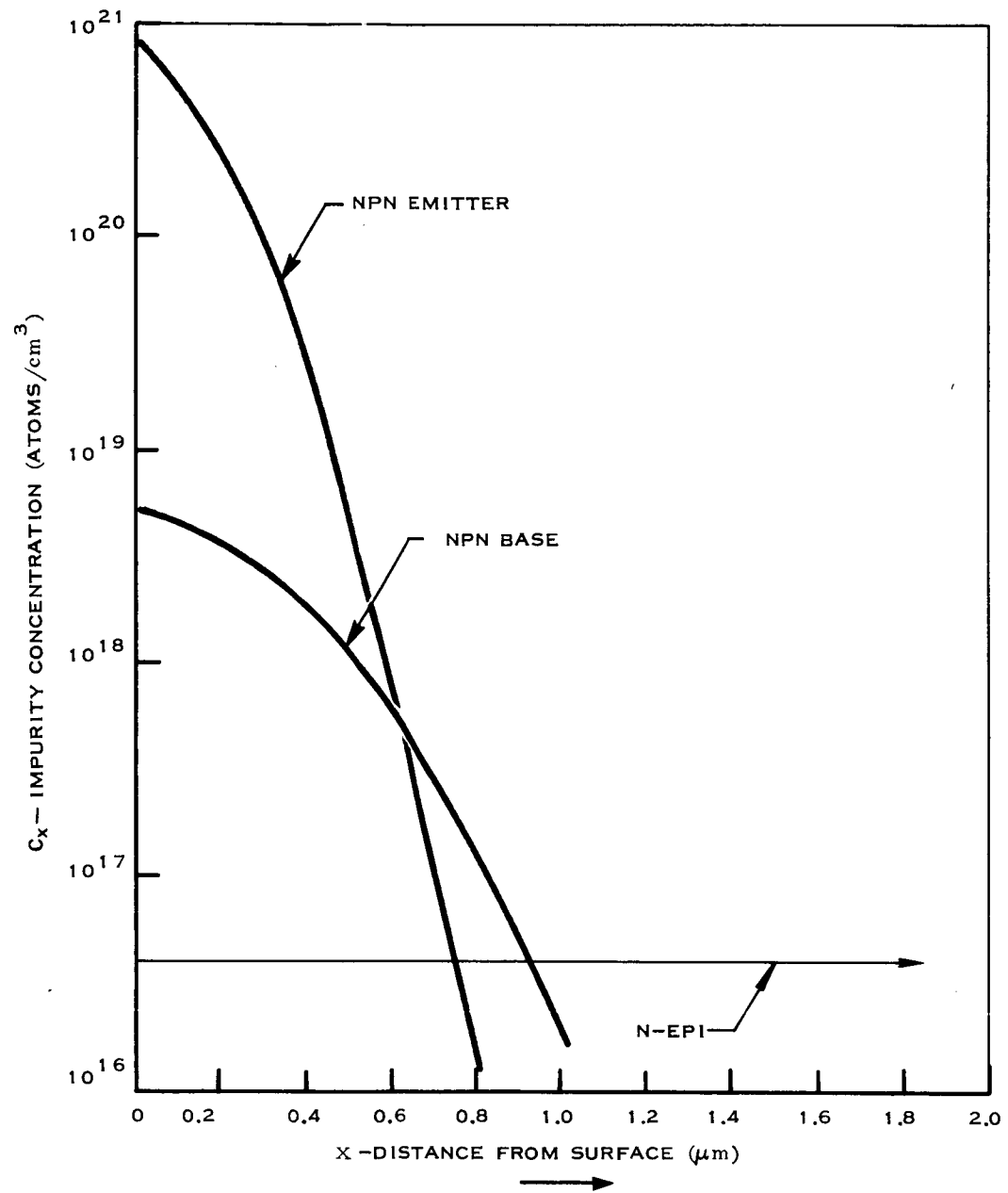
Figure 11.   Buried-Layer NPN Transistor Impurity Profile
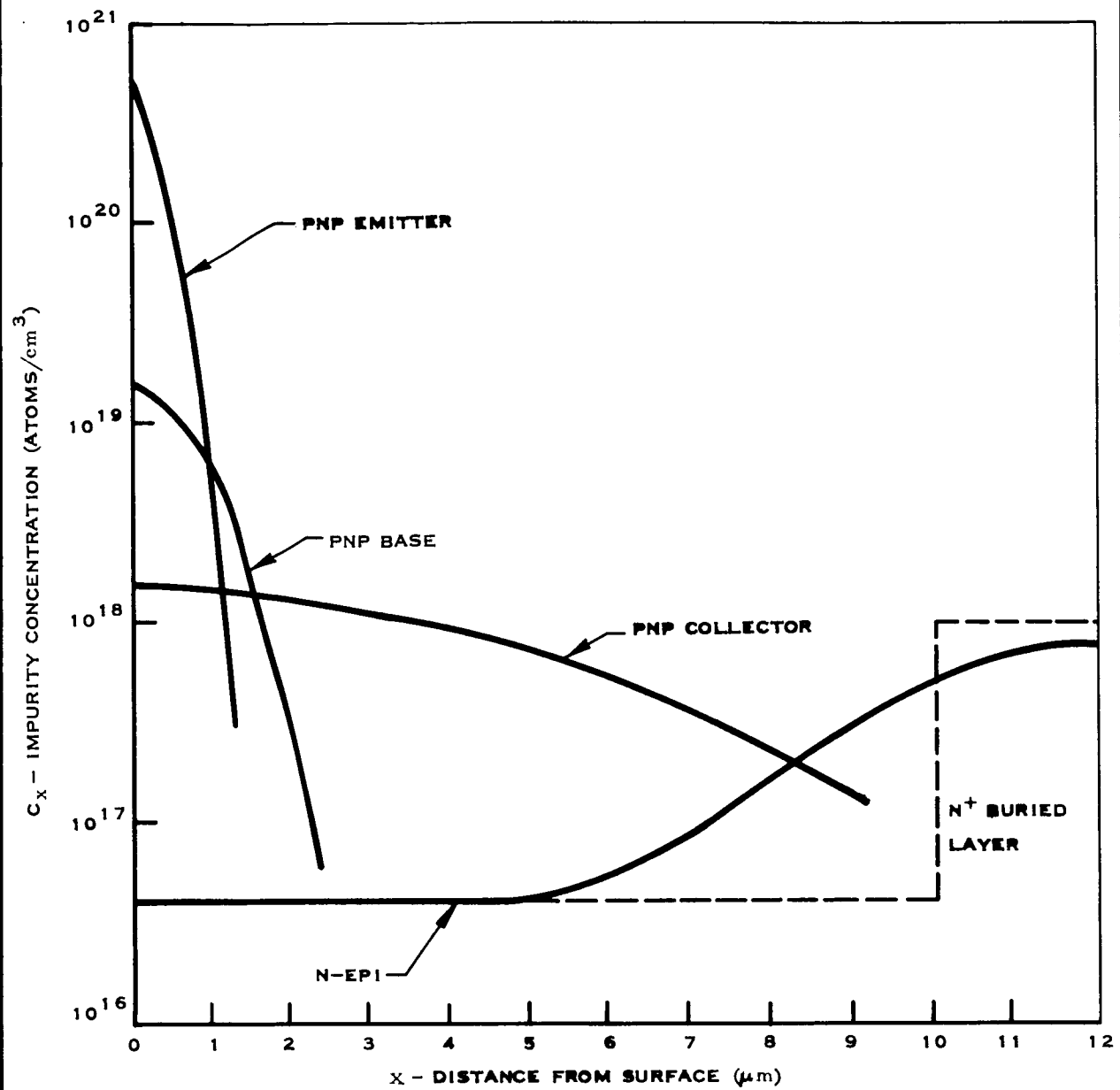
Figure 12.   Buried-Layer PNP Transistor Impurity Profile
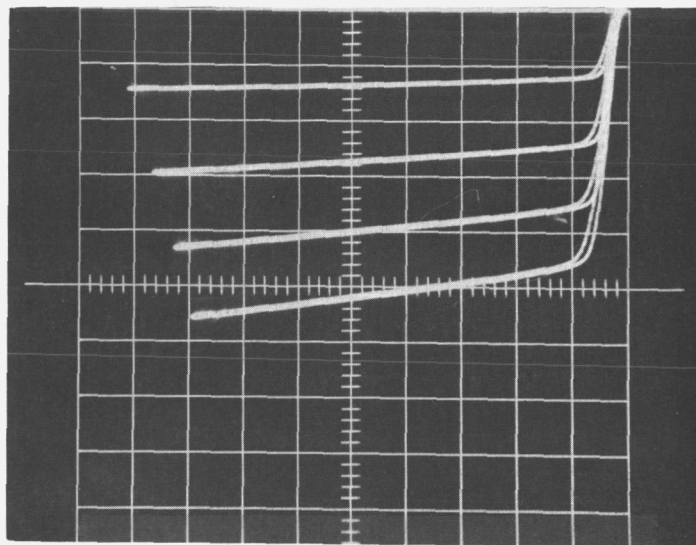
(a.) PNP No. 33

I_B = 10 μA/STEP
HORIZONTAL = 0.5 V/DIV
VERTICAL = 500 μA/DIV
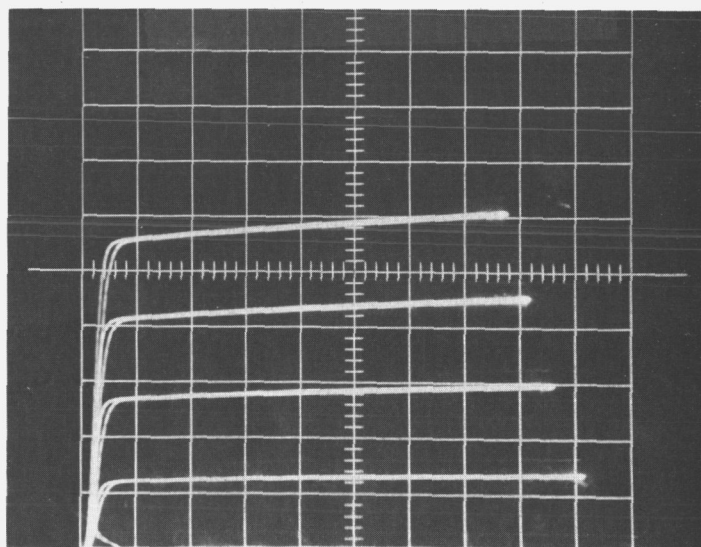
(b.) NPN No. 33

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Figure 13.   Complementary Transistor Pair—Schedule A Process
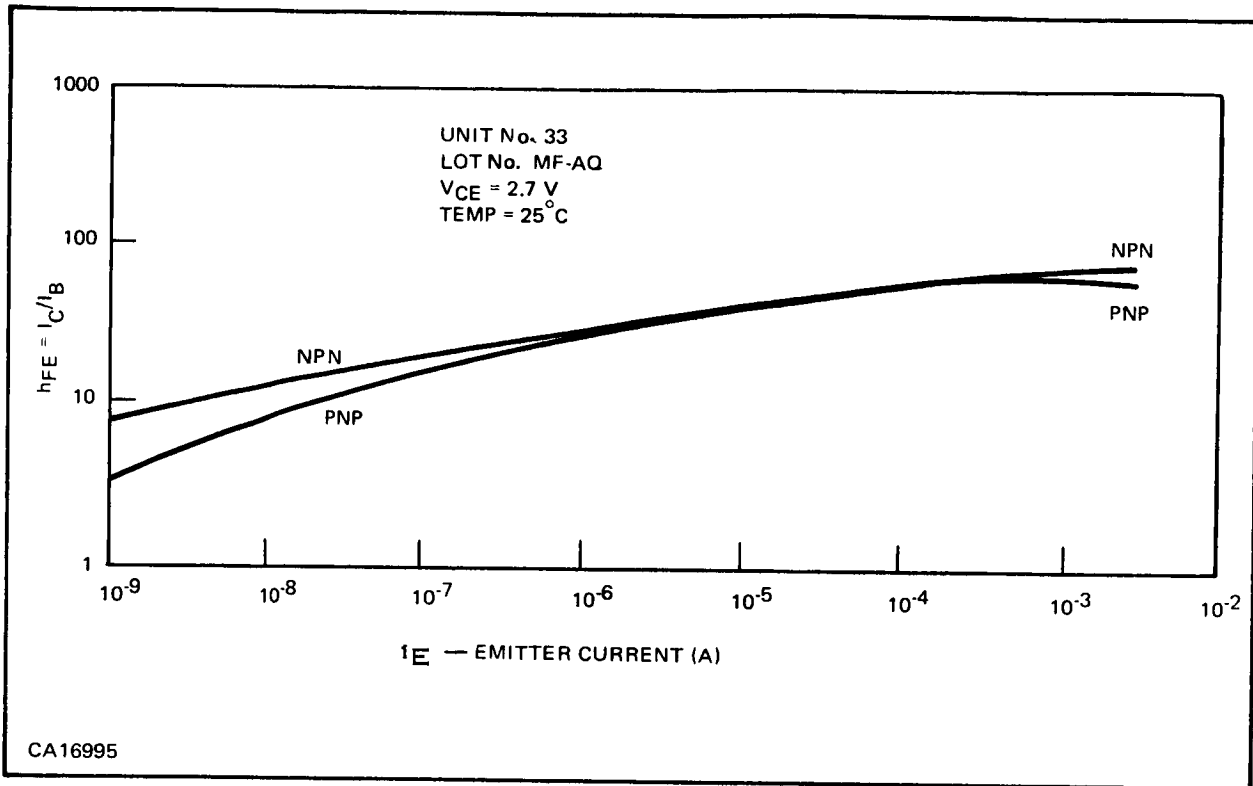
Figure 14. h_{FE} versus I_E—Schedule A Process

deposition and diffusion will be performed into the region of the "buried layer" where the PNP collector will be formed, and also into the region where the P-N junction isolation will be formed. The slices then receive the required epitaxial layer. Slices are next placed in a furnace until the P-type impurity reaches the epitaxial surface. This results in a retrograded P-type collector and P-N junction isolation.

The remainder of the process is similar to the previously mentioned process. The cross-sectional view is seen in Figure 16. The resulting profile for the PNP transistor is approximately that of Figure 17. The profile of the NPN is basically the same as that of Figure 11, with the exception that the buried N^+ layer is closer to the collector-base junction.

This process was initiated to produce a more consistent base (PNP) diffusion, resulting in better yields. The lower concentration of the PNP collector near the surface allows higher BV_{CEO} for the same h_{FE} and reduced collector-base capacitance. This collector profile acts in much the same way as a "buried-layer" structure. Concentration at the surface is low, and the concentration below the surface is progressively higher. Since this reduces the need for the relatively deep collector junction, the epitaxial layer can be reduced ($\approx$ 5 μm). This leaves the "buried-layer" region under the NPN closer to the active region of the NPN device and thus reduces the $V_{CE(sat)}$ of this device.

Figure 18 shows the curve tracer results of a typical complementary pair of transistors using Schedule B. Some characteristic data on a typical unit are given in Figure 19 (h_{FE} versus I_E), and in Figure 20 (f_t versus I_E).
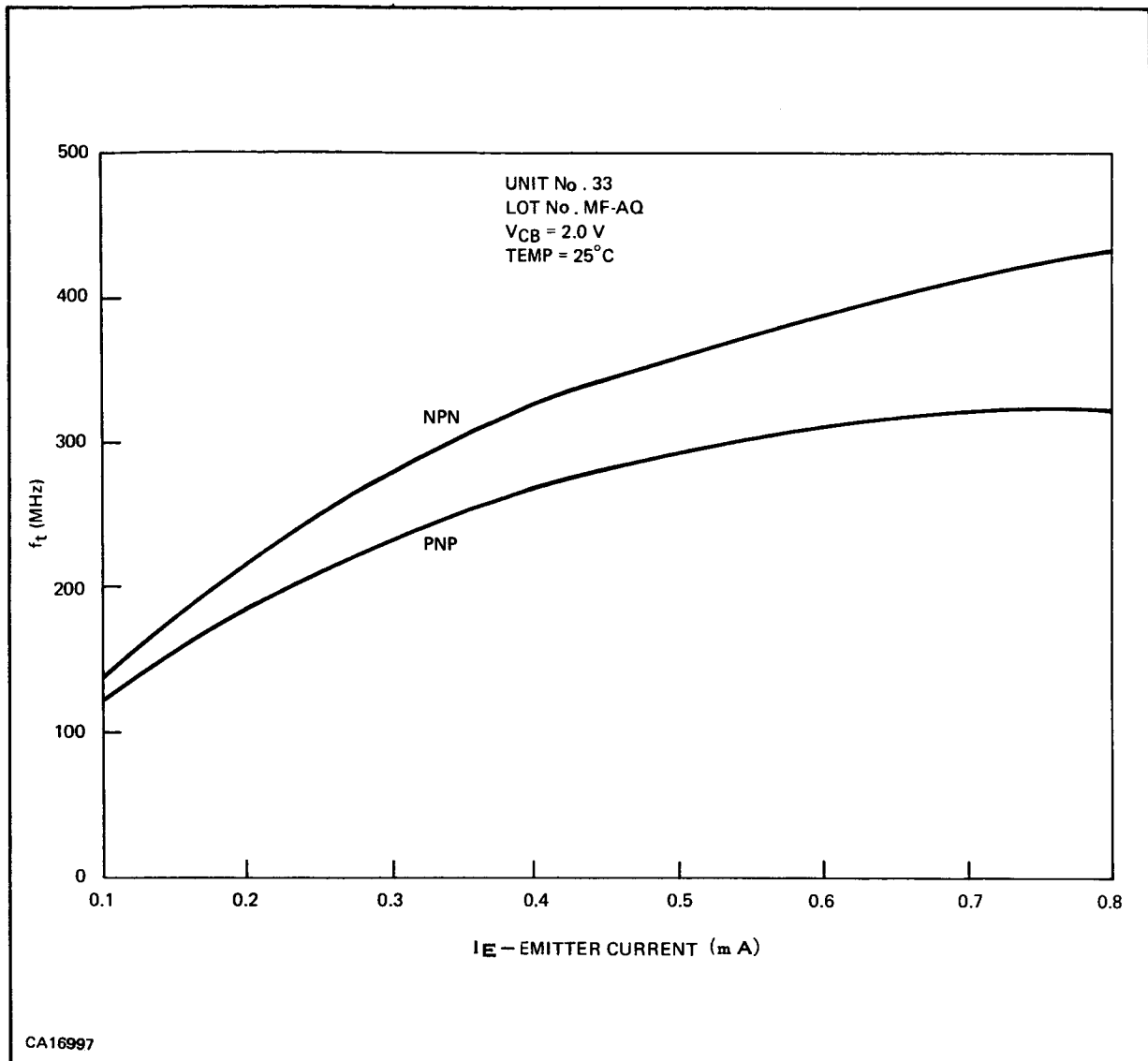
Figure 15. f_t versus I_E—Schedule A Process

Although a limited effort has been made in developing this process, we feel that it has some definite advantages, primarily in the ease of fabrication.

4. Schedule Comparison

The NPN transistor should be basically the same for both schedules, because the same profile is used. The $V_{CE(sat)}$ of Schedule B's NPN transistor is somewhat lower because the buried layer has been moved closer to the collector-base junction.

The PNP devices fabricated on both schedules had basically the same properties. It was noticed that the f_t of the Schedule B material was somewhat lower and this was possibly due to the retrograded collector.

31
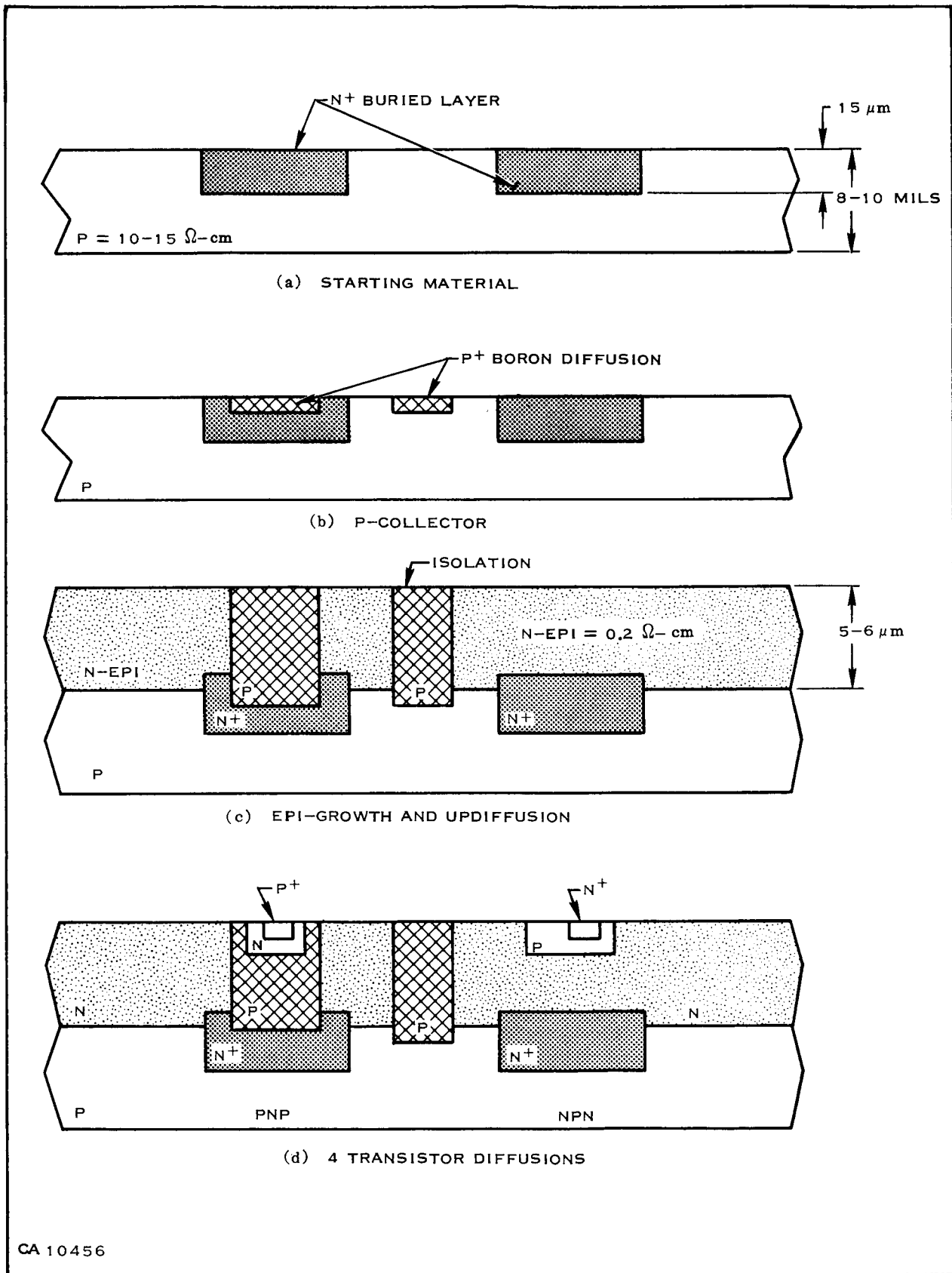
Figure 16.   All-Diffused PN Junction Isolated Double Buried Layer—Schedule B Process
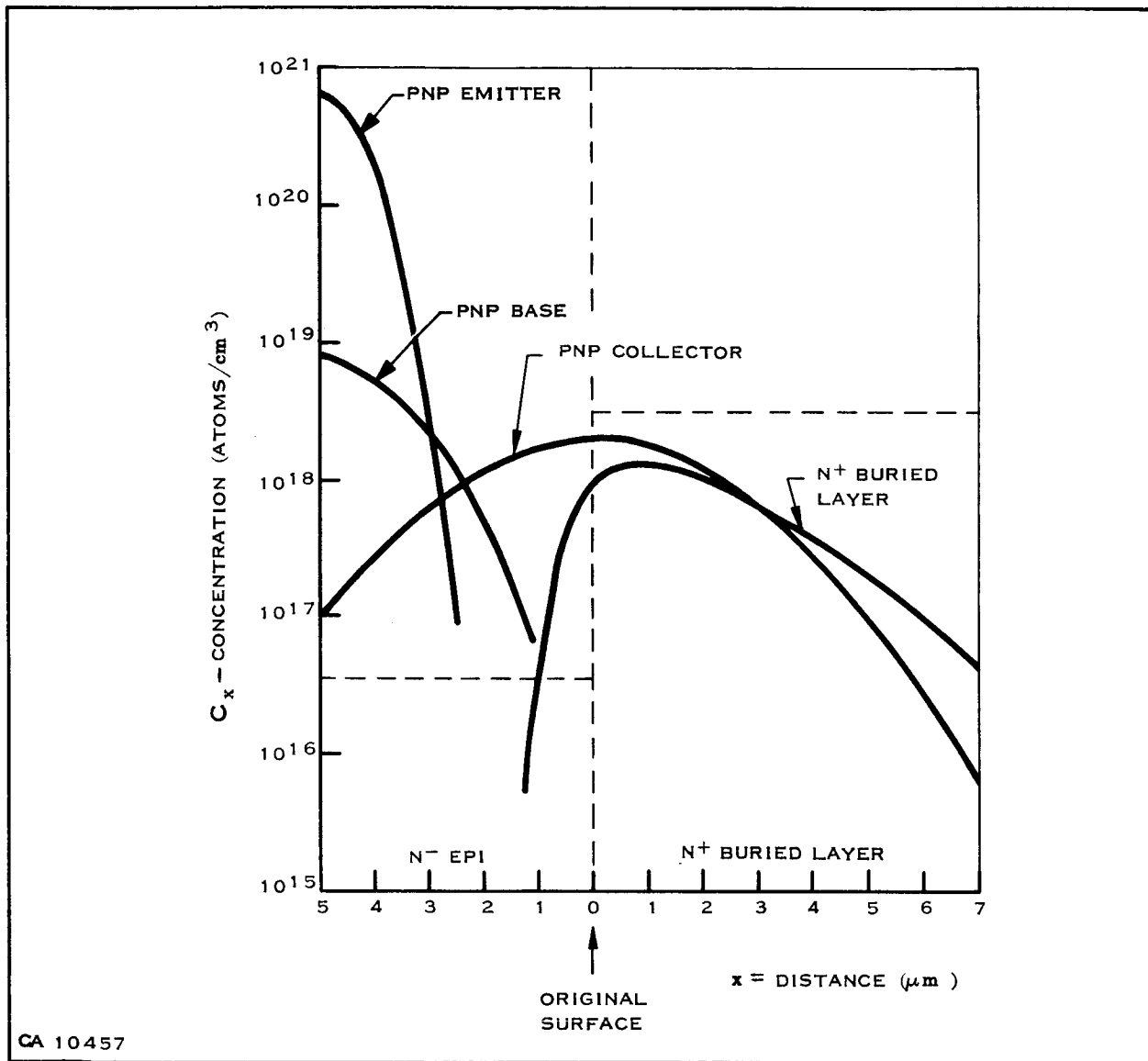
Figure 17.   Double Buried-Layer PNP Transistor Impurity Profile

The main purpose of the two schedules was to produce a more consistent PNP device and thus increase yield. Not enough B material was processed to allow a direct statement to this effect, but of those slices tested, the h_{FE} had less variation across the slice using the Schedule B approach than with the Schedule A material.

The two approaches require the same amount of processing steps and differ only as to when they are performed in the schedule. Schedule B does require that when the material is etched before the epitaxial layer is applied, a set amount of the parent material be removed. This step could result in a potential problem area and cause inconsistency.
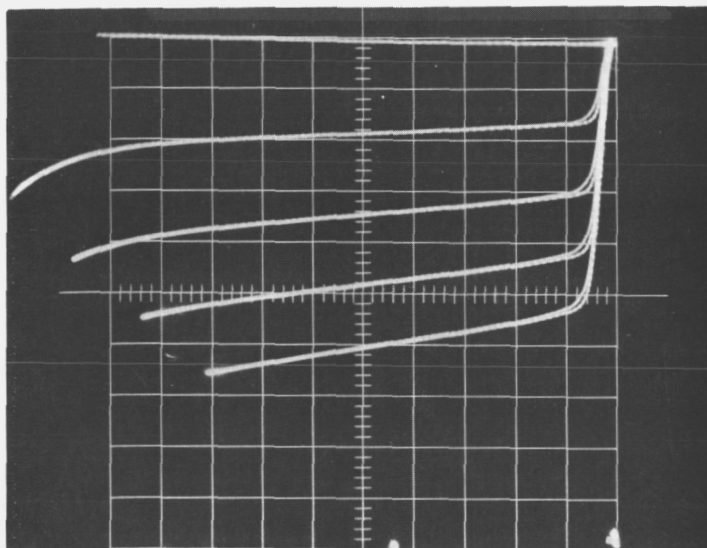
(a.) PNP No. 43

I_B = 10 μA/STEP
HOR = 0.5 V/DIV
VERT = 500 μA/DIV
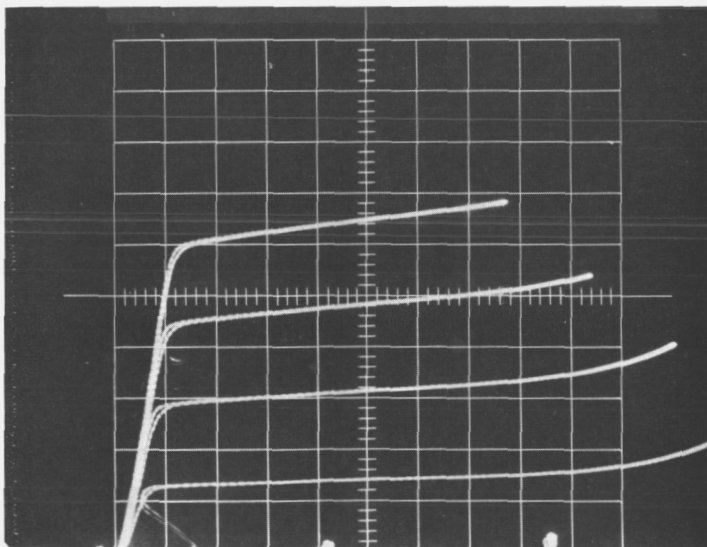
(b.) NPN No. 43

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Figure 18. Complementary Transistor Pair—Schedule B Process
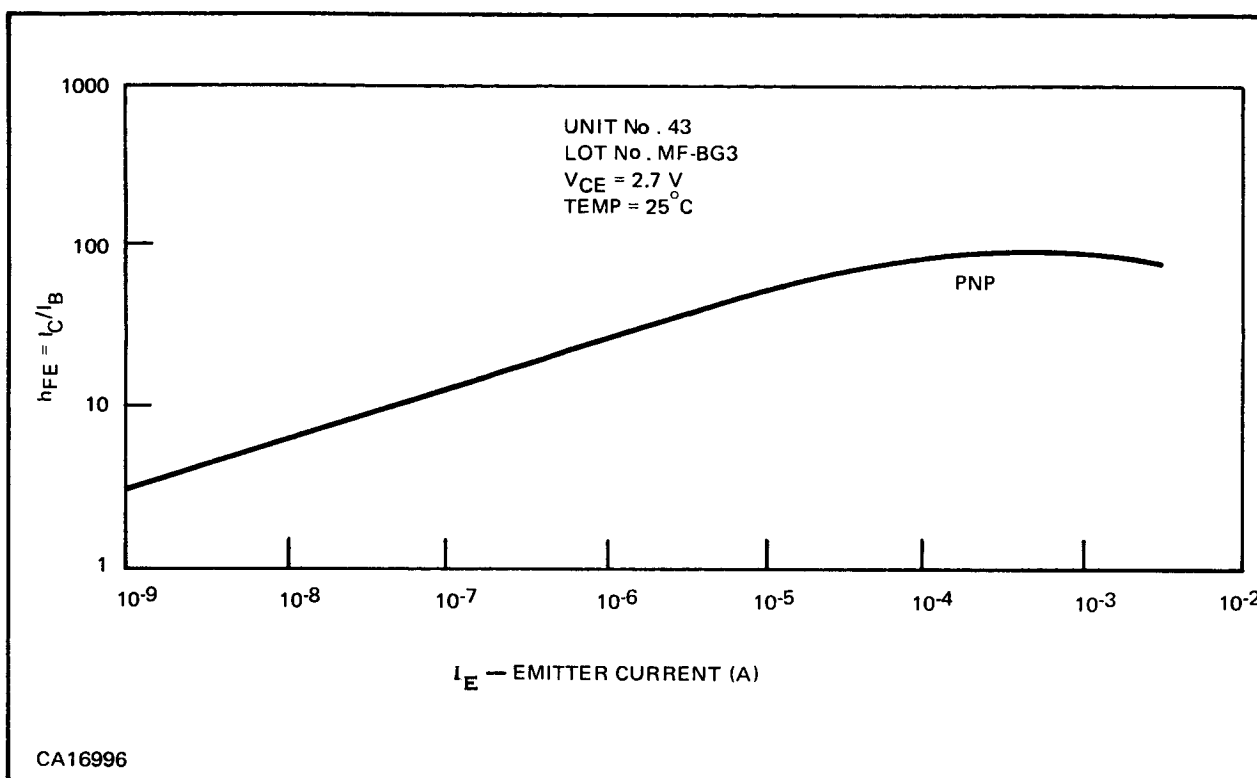
Figure 19. h_{FE} versus I_E—Schedule B Process
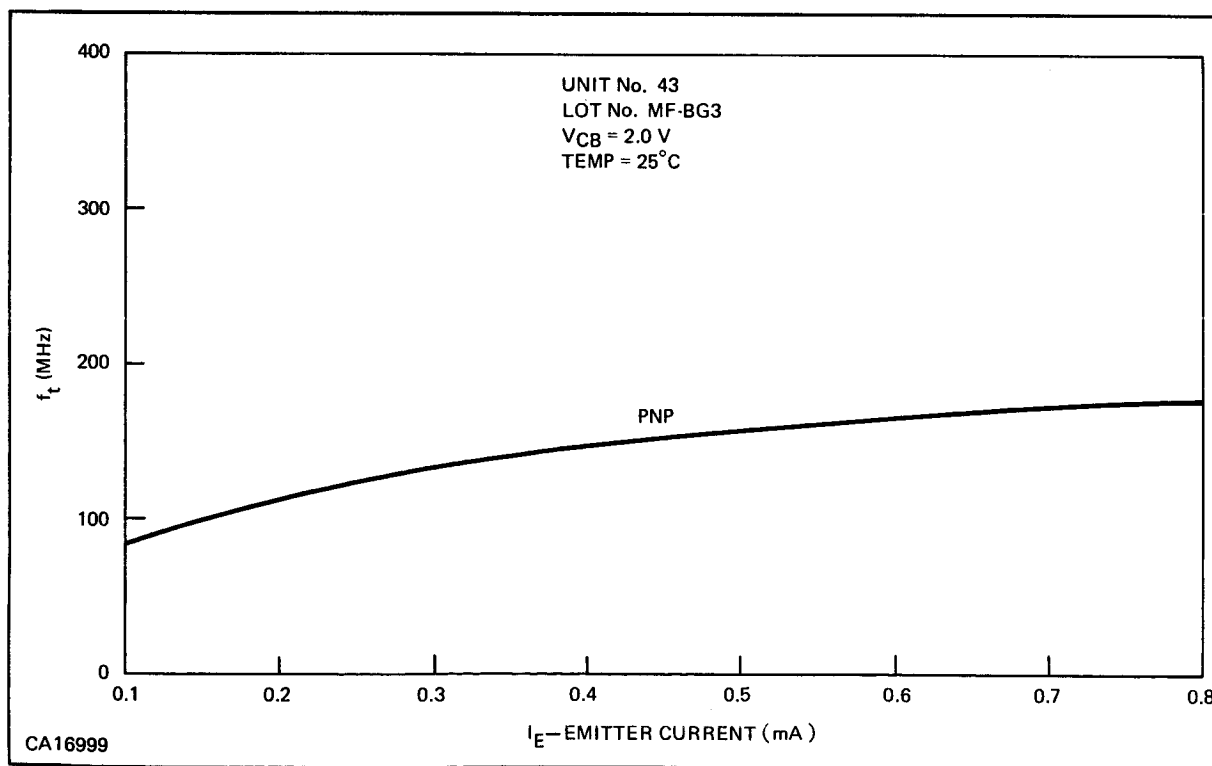
Figure 20. f_t versus I_E—Schedule B Process

E. BAR DESIGN

1. Device Geometry

The transistor geometry used in this contract was common for all transistors except the multi-emitter input transistor. The geometry shown in Figure 21 is basically a 0.7×0.7 mil^2 emitter with a single base contact and collector guard ring.

The geometry used for the multi-emitter input transistor, shown in Figure 22, is basically a 0.4×0.4 mil^2 emitter with a base resistor and collector guard ring. The base resistor is used to reduce emitter-to-emitter current gain.

Resistor geometry is shown in Figure 23. The resistor is 0.3-mil wide and has a nominal sheet resistance (R_s) of 550 $\Omega/\square$. It is fabricated using the diffusion for the NPN base. The temperature coefficient for the diffused resistor (TCR) is given in Figure 24. The proper TCR is a very important parameter in micropower complementary logic circuits. The choice of a proper coefficient will compensate for h_{FE} variation with temperature [See Equation (1)] and allow for worst-case power to occur at 25°C.

EMITTER: $0.7 \times 0.7 \text{ MIL}^2$
EMITTER CONTACT: $0.3 \times 0.3 \text{ MIL}^2$
BASE: $1.9 \times 1.3 \text{ MIL}$
BASE CONTACT: $0.3 \times 0.7 \text{ MIL}^2$
COLLECTOR: $3.7 \times 3.1 \text{ MIL}^2$
BURIED LAYER: $4.7 \times 4.1 \text{ MIL}^2$

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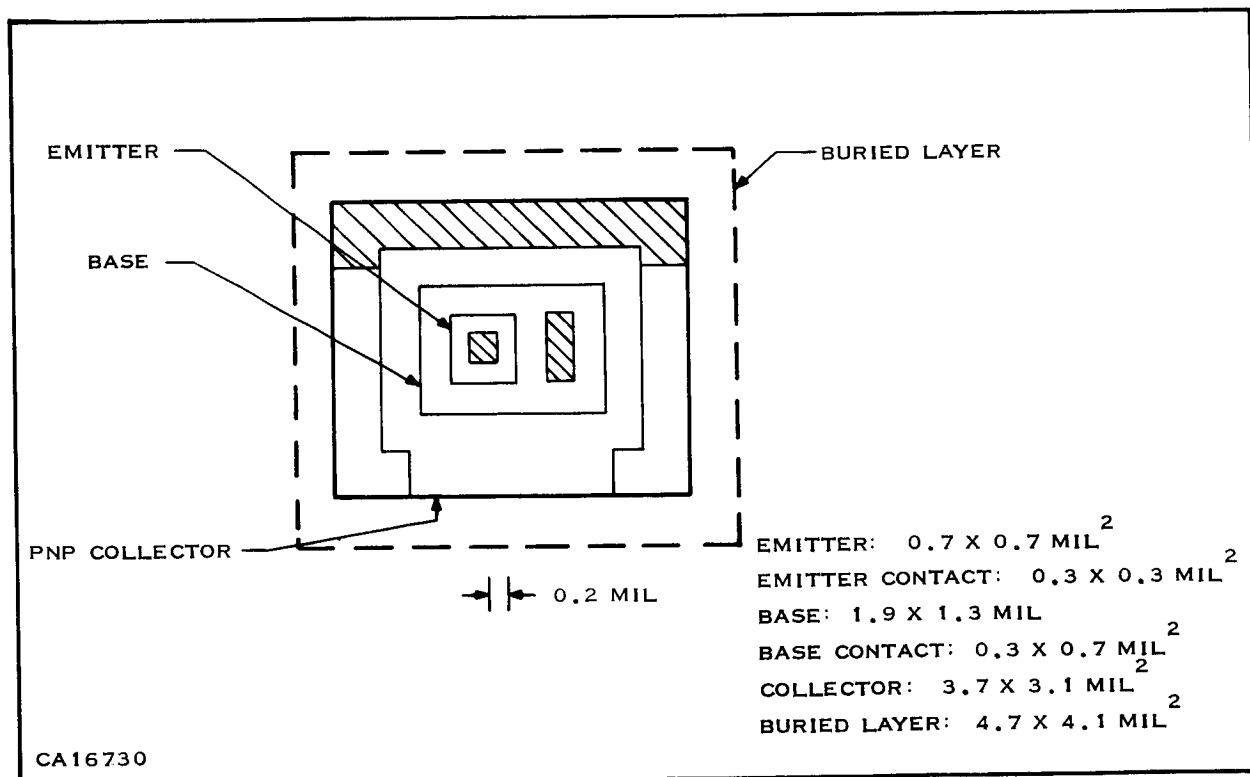
Figure 21.   Output Transistor Geometry

EMITTER $= 0.4 \times 0.4 \text{ MIL}^2$

EMITTER CONTACT $= 0.25 \times 0.25 \text{ MIL}^2$

BASE $= 2.3 \times 2.4 \text{ MIL}^2$

COLLECTOR $= 6.3 \times 7.5 \text{ MIL}^2$

0.2 MIL

CA16731
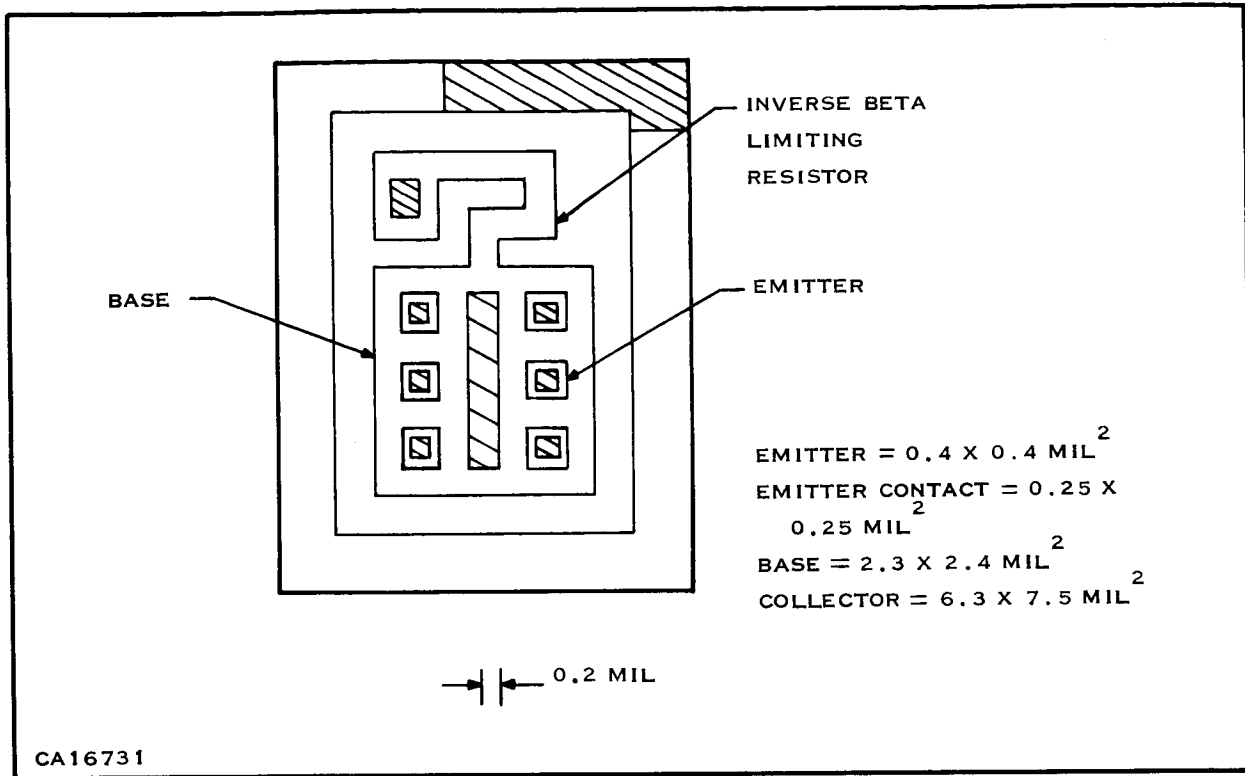
Figure 22.　Multi-Emitter Transistor Geometry

0.2 MIL

$R_S \approx 550 \ \Omega/\square$

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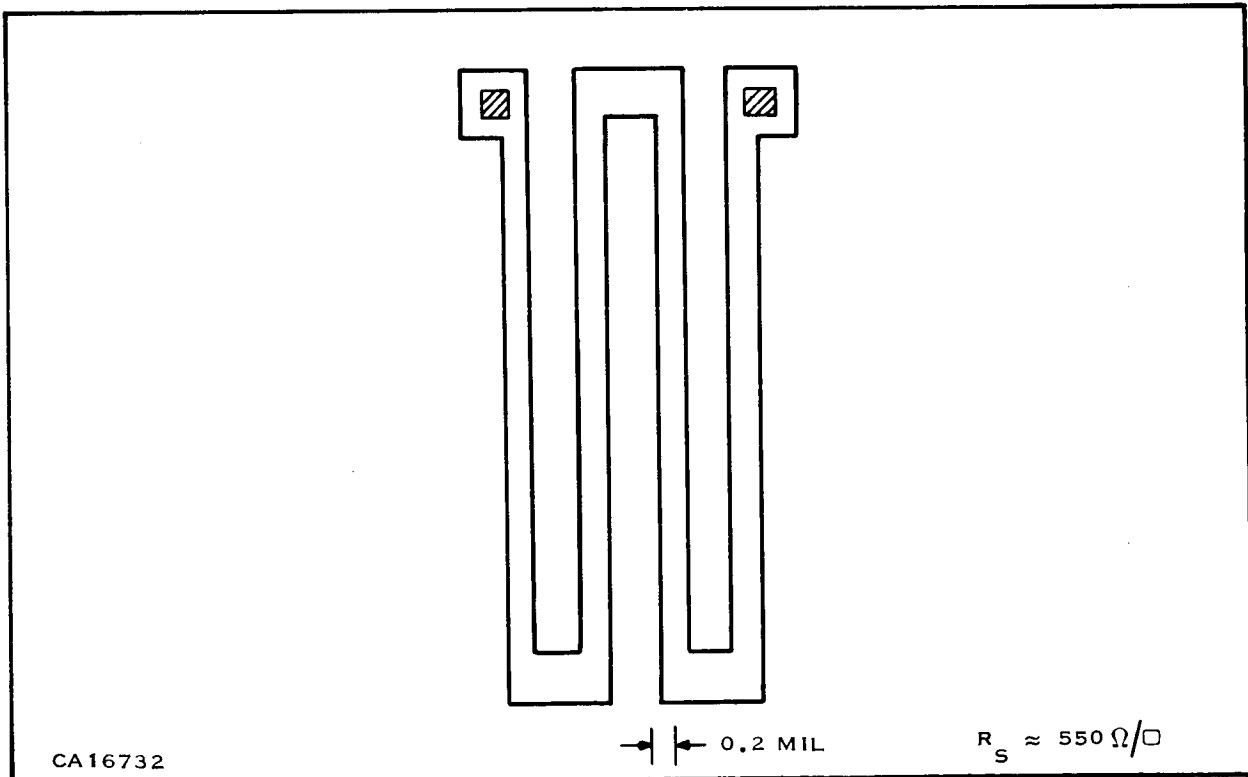
Figure 23.　Resistor Geometry
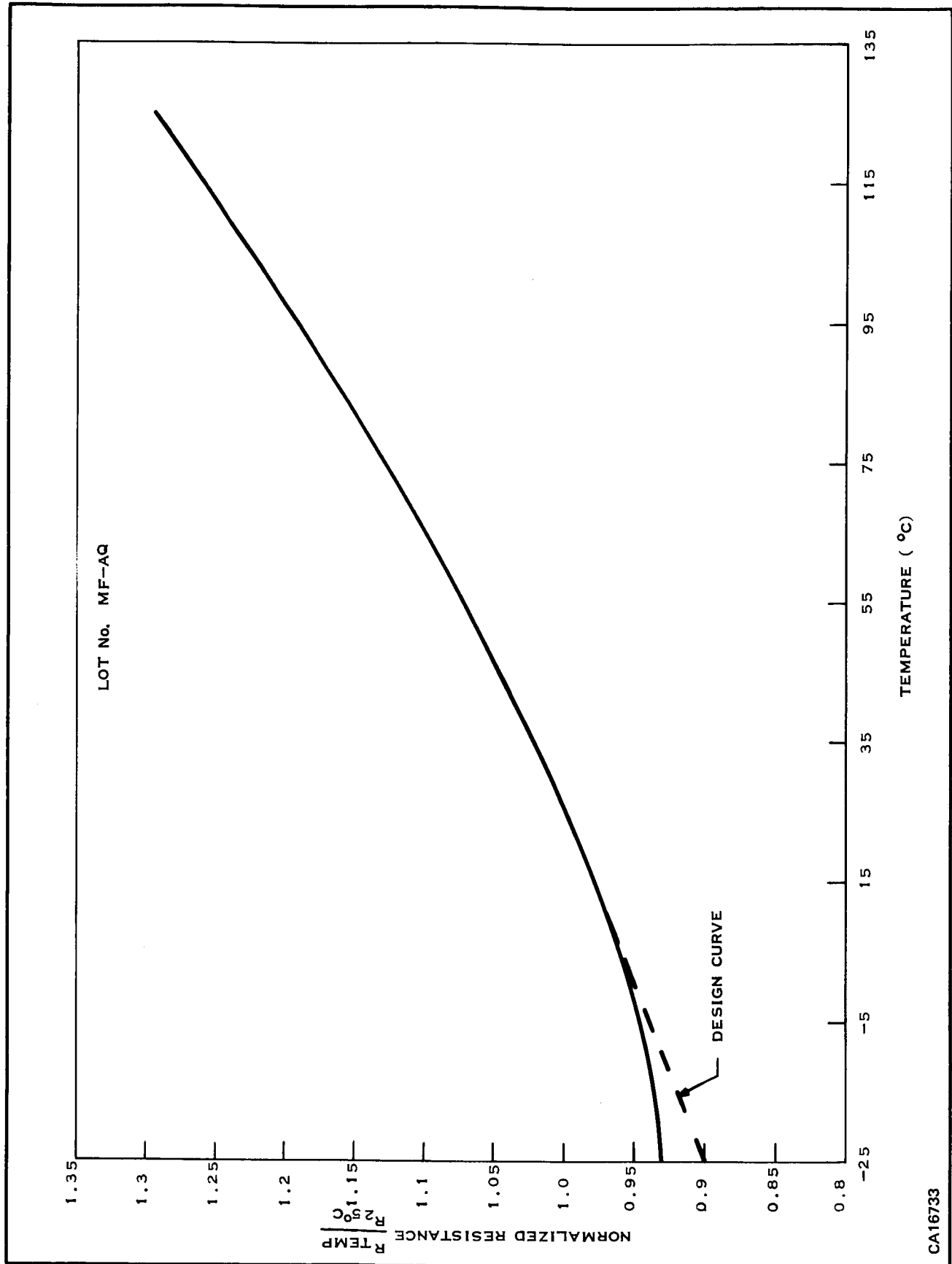
Figure 24. Diffused Resistor Temperature Coefficient (TCR)

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The capacitor geometry is shown in Figure 25. The capacitor is fabricated using the N^+ buried-layer and NPN emitter diffusion connected in parallel to form the N region. The P region is the PNP collector diffusion. The capacitance-versus-voltage plot is given in Figure 26. Capacitor designations refer to Figure 7.

2. Master Bar Approach

The three required circuits, single-6 input NAND gate, dual-3 input NAND gate, and J-K Flip-Flop, were fabricated using the master bar approach. That is, all circuits had a common bar
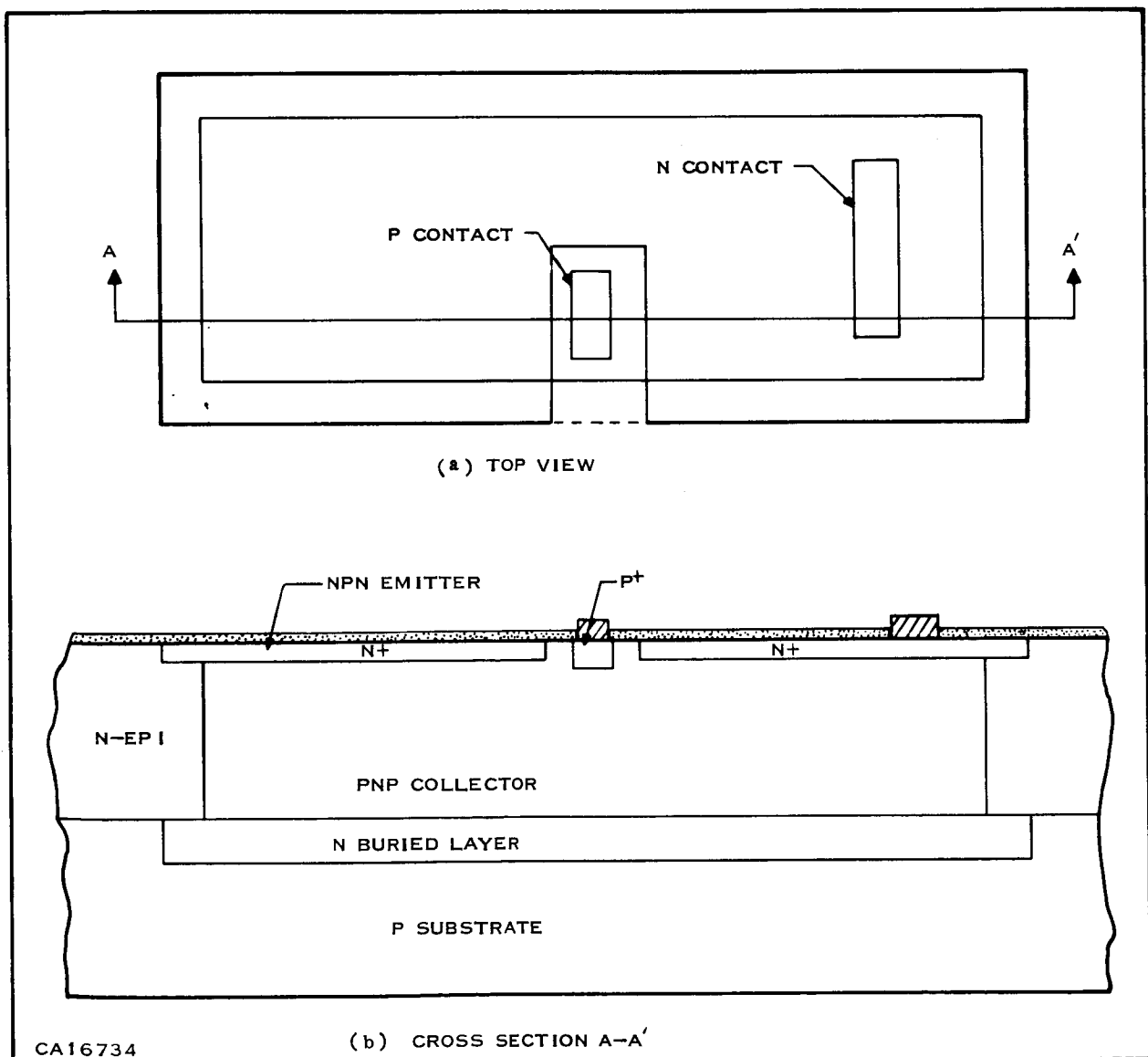
Figure 25. Diffused Capacitor Geometry
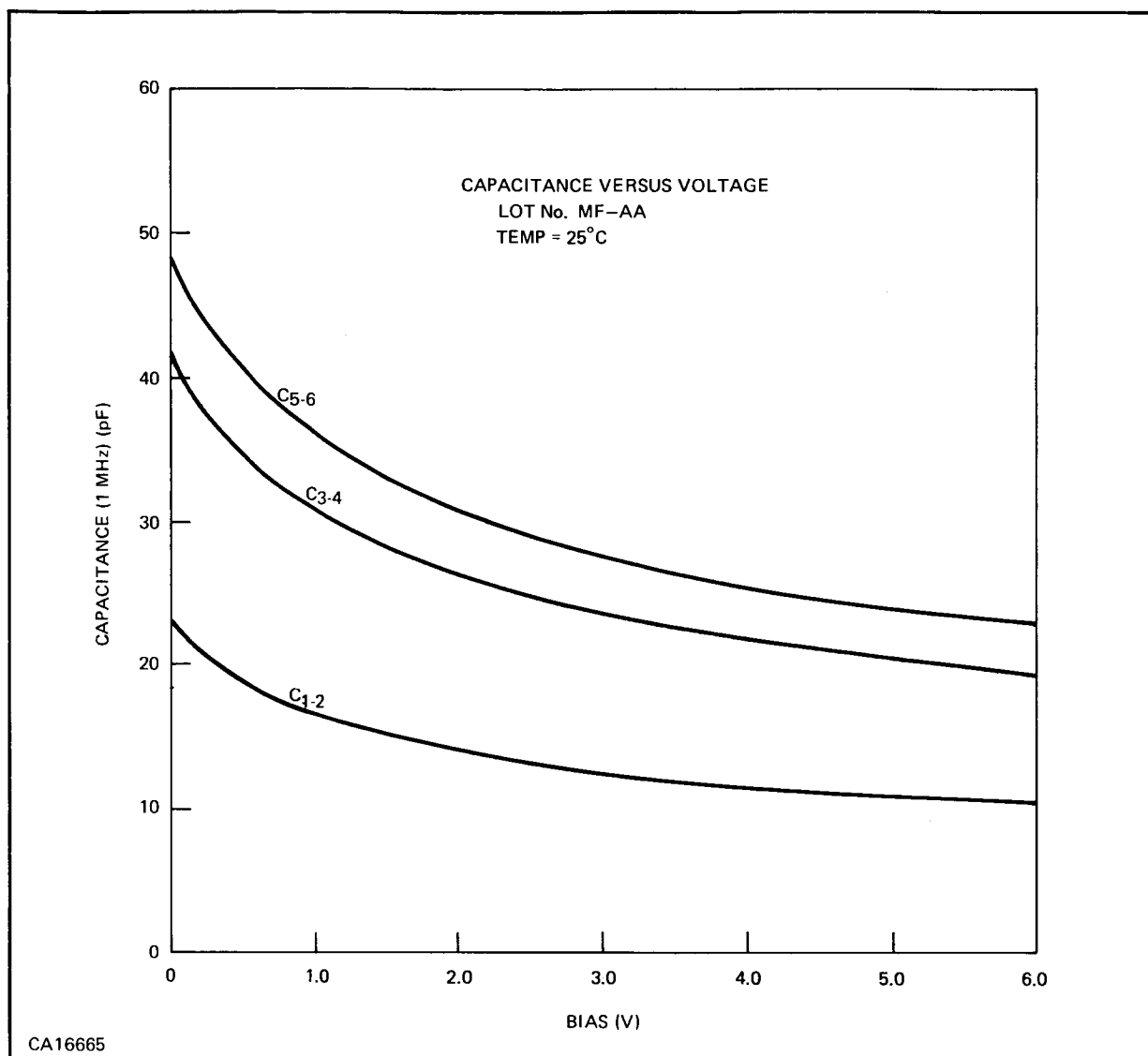
Figure 26. Capacitor Voltage Characteristic

layout, with circuit configuration determined by the metallization pattern. The master-bar layout is shown in Figure 27. Metallization patterns are:

1)   Single-6 NAND gate—Figure 28.

2)   Dual-3 NAND gate—Figure 30.

3)   J-K Flip-Flop—Figure 32.

Photographs of completed circuits are shown as Figures 29, 31, and 33.

FOLDOUT FRAME

FOLDOUT FRAME

0.002 IN

Figure 27. Master Bar Layout

41

FOLDOUT FRAME 1

FOLDOUT FRAME 2

Figure 28. Single-6 NAND Gate

CA16923

43

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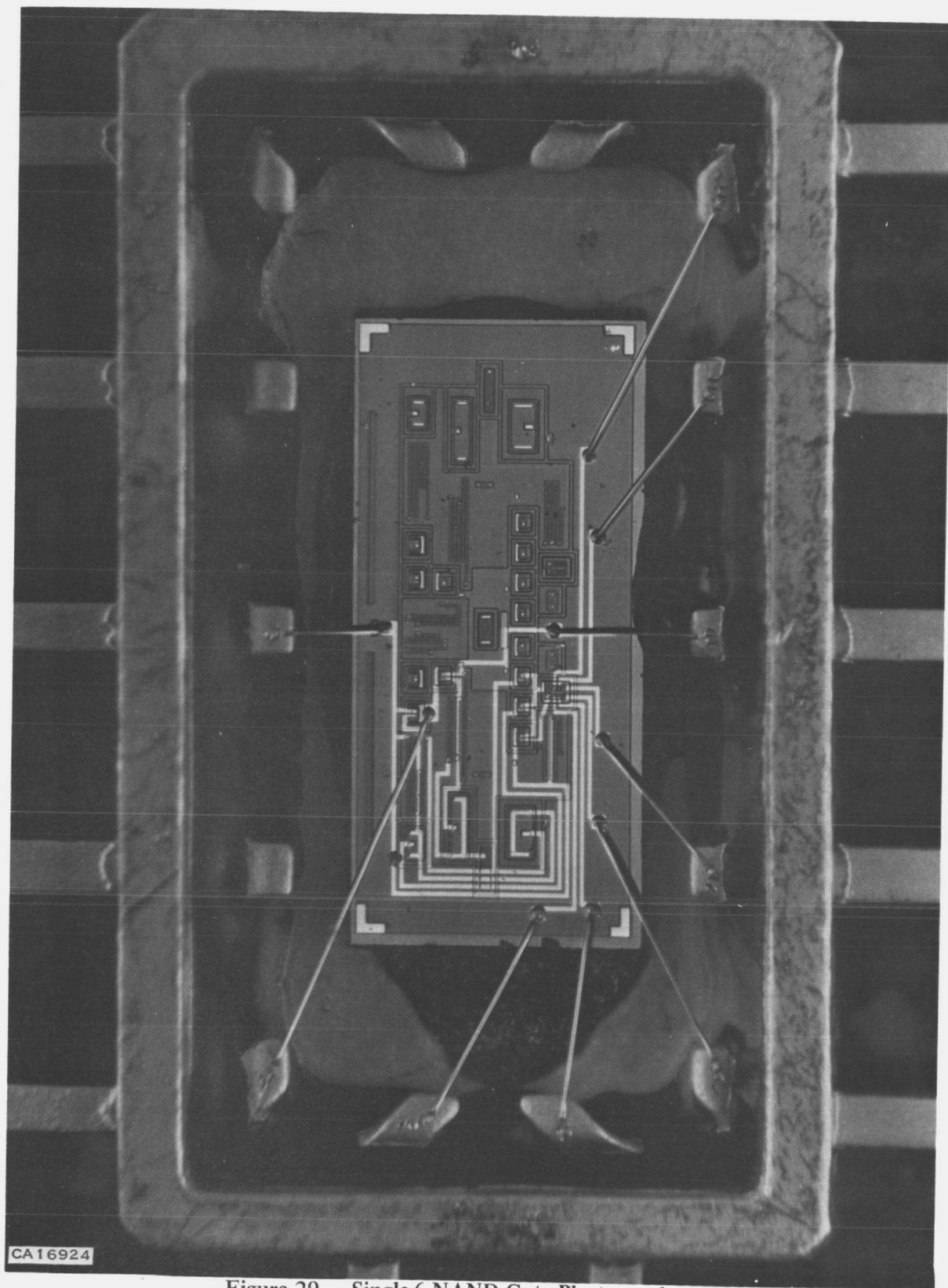
CA16924

Figure 29.   Single-6 NAND Gate Photograph
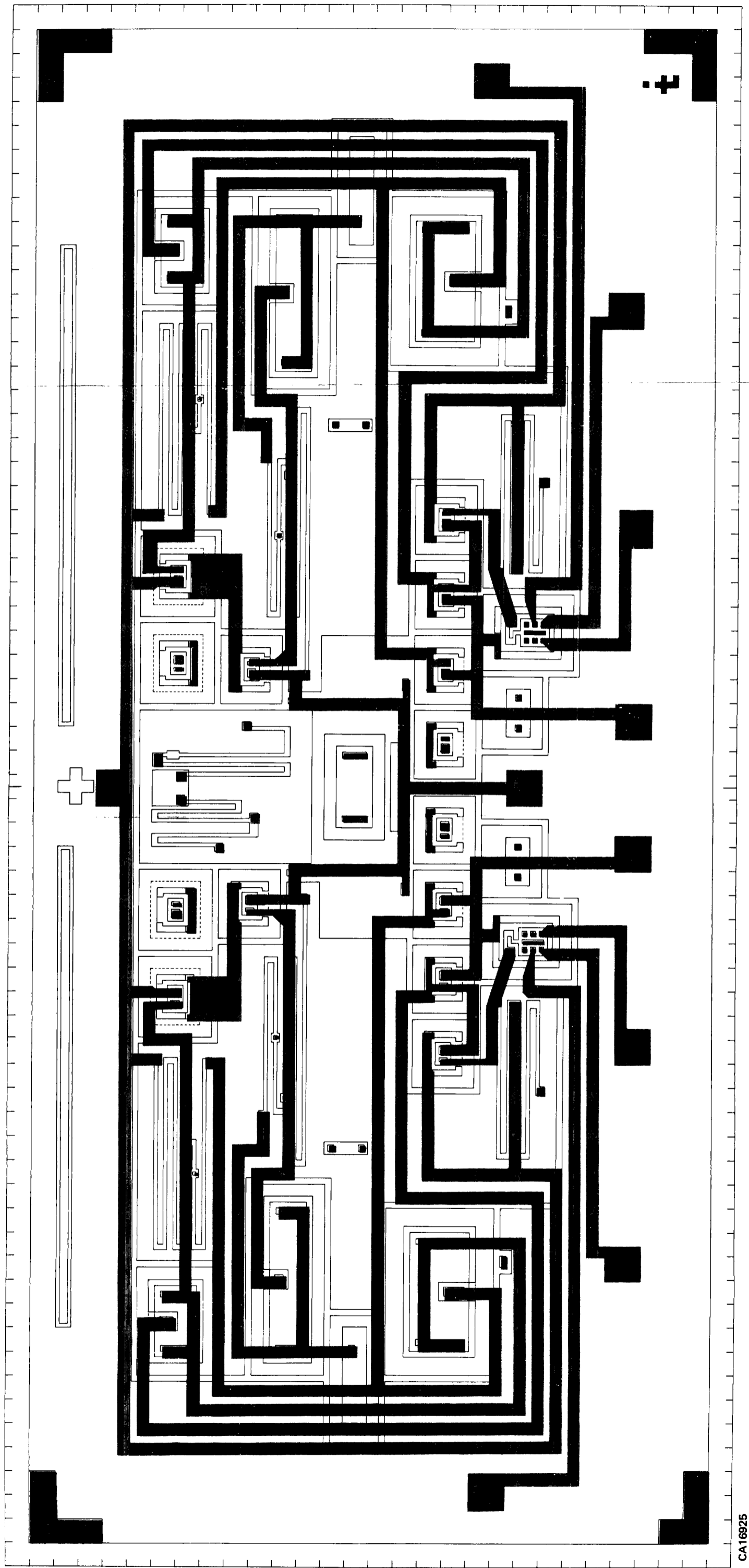
Figure 30. Dual-3 NAND Gate

FOLDOUT FRAME 2

FOLDOUT FRAME 1

CA16925

47
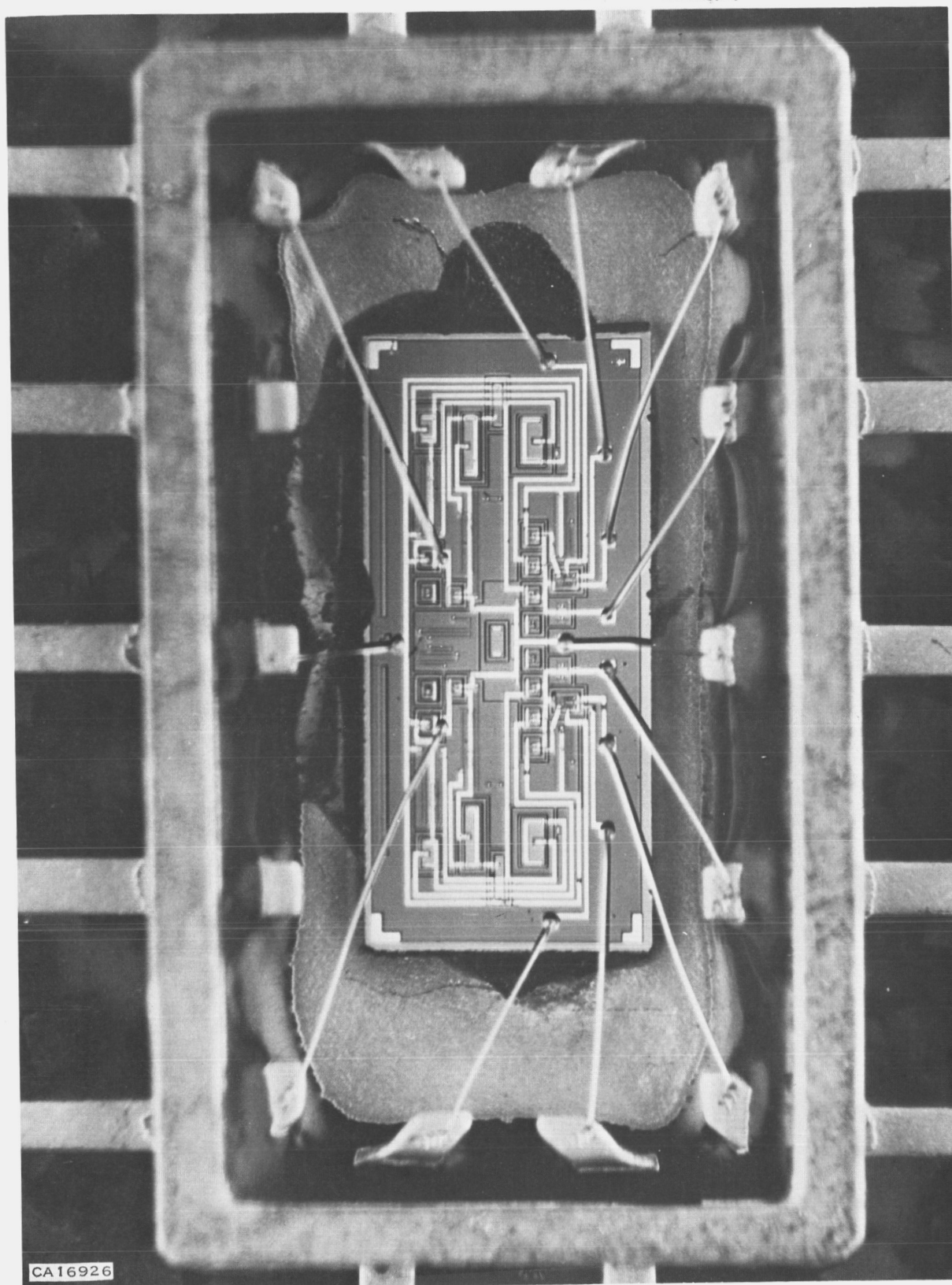
Figure 31.   Photograph of Dual-3 NAND Gate
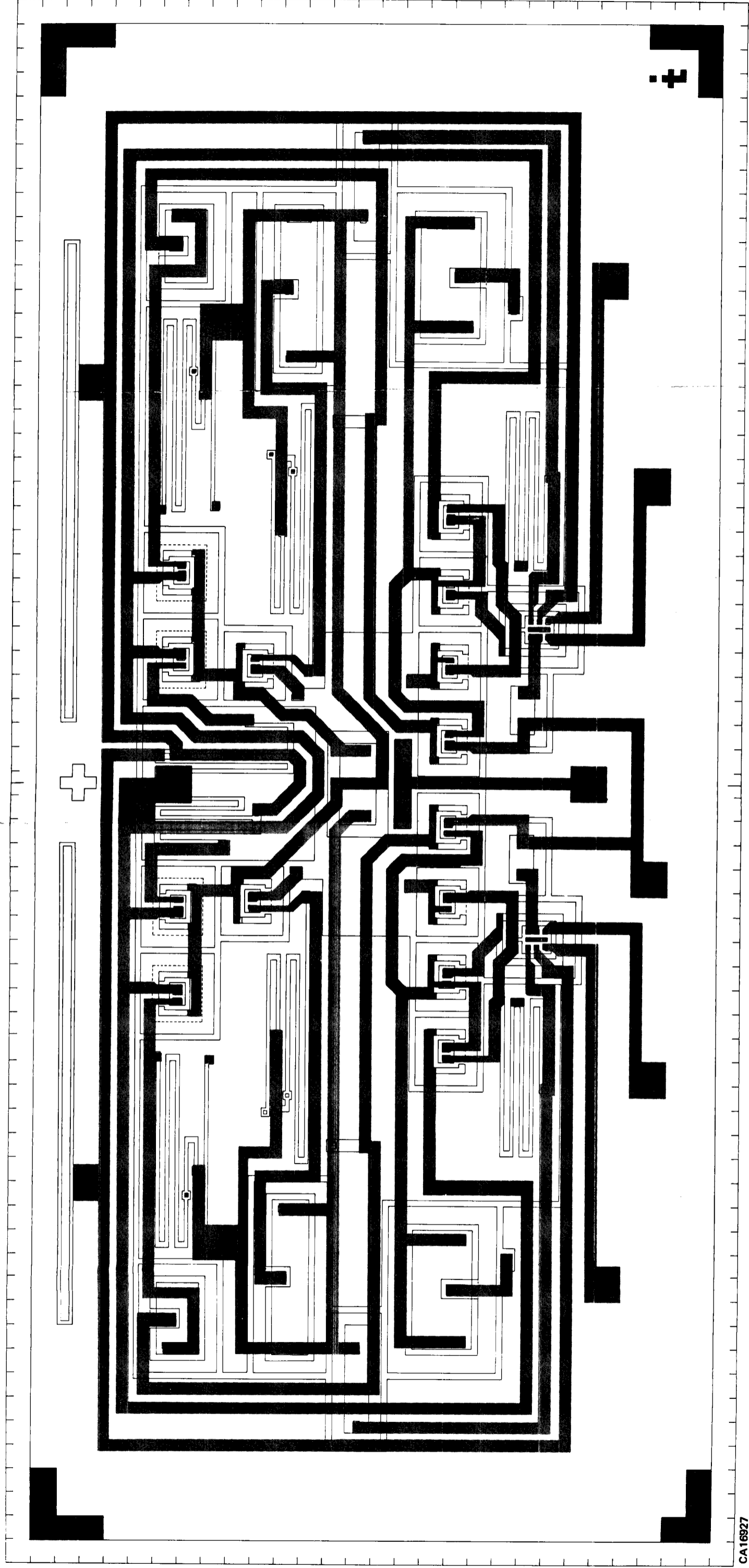
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FOLDOUT FRAME 1

FOLDOUT FRAME 2

Figure 32. J-K Flip-Flop

51
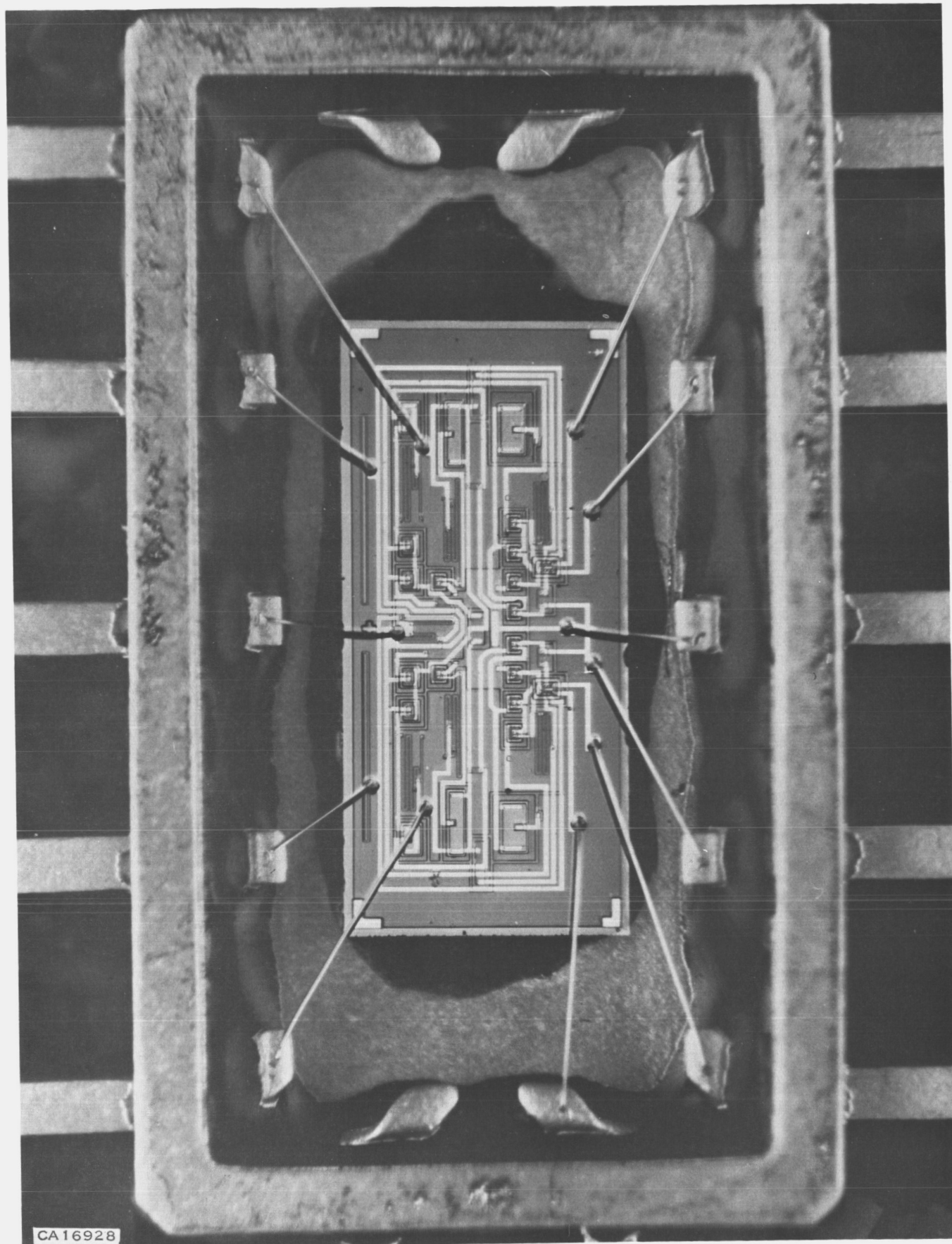
CA16928

Figure 33.   Photograph of J-K Flip-Flop

The completed circuits were mounted and bonded in a 14-lead flat package. The bonding diagrams are:

1) Single-6 NAND gate—Figure 34.

2) Dual-3 NAND gate—Figure 35.

3) J-K Flip-Flop—Figure 36.

F. CIRCUIT CHARACTERIZATION

1. Introduction

The purpose of this section is to present the typical characteristics of the circuits fabricated under this contract. Eighteen separate tests were used for the NAND gates and 12 tests for the Flip-Flops. This large number of tests is necessary to describe the circuits completely. Because of the large number only a few circuits of each type were selected for testing. In this selection an effort was made to choose a representative sample. For example, one of the NAND gates tested had relatively low h_{FE} output transistors. Some of the circuits fabricated on the contract had higher operating frequencies while others were lower standby-power units. Therefore, the data plots presented here can be taken as average operating characteristics.

The basic characterization "setup" for the circuits is shown in Figure 37. The drive gate was a breadboard using discrete devices. The capacitance at the output due to the test setup at NO LOAD was approximately 15 pF.

Circuits were fabricated using both Schedule A and Schedule B processes. The major emphasis here will be placed on Schedule A performance with the more important parameters being shown for Schedule B later in this section.

2. NAND Gate Characterization-Schedule A Process

NAND gate characterization on the single-6 input NAND gate will be presented since it will indicate "worst-case" power. The dual-3 NAND gate should have identical input and output characteristics. In general the dual-3 circuits tested have characteristically lower F_{max} and lower worst-case standby power. The slower speeds are due in a large part to the required expander input.

The method of specifying transient performance of the NAND gates will be to quote the delay, rise, and fall times.[3]

Propagation delay time (t_p) is defined as the average of the delays for both the leading and trailing edges of the input voltage pulse. Using the waveforms of Figure 38, the following definitions will apply: The leading-edge delay (t_{d0}) is the time difference between that time when the input pulse reaches 50 percent of its final value and the time when the output of the gate has fallen to its 50 percent point. Similarly, the trailing-edge delay (t_{d1}) is defined as the time between the 50 percent points, with the input-pulse trailing edge as reference. The propagation delay is then the average of t_{d0} and t_{d1}, that is $t_p = (t_{d0} + t_{d1})/2$.

Figure 34.   Single-6 NAND Gate Bonding Diagram (Top View)

CA16929

$$Y = \overline{ABCD}$$
$$(D = EXP)$$
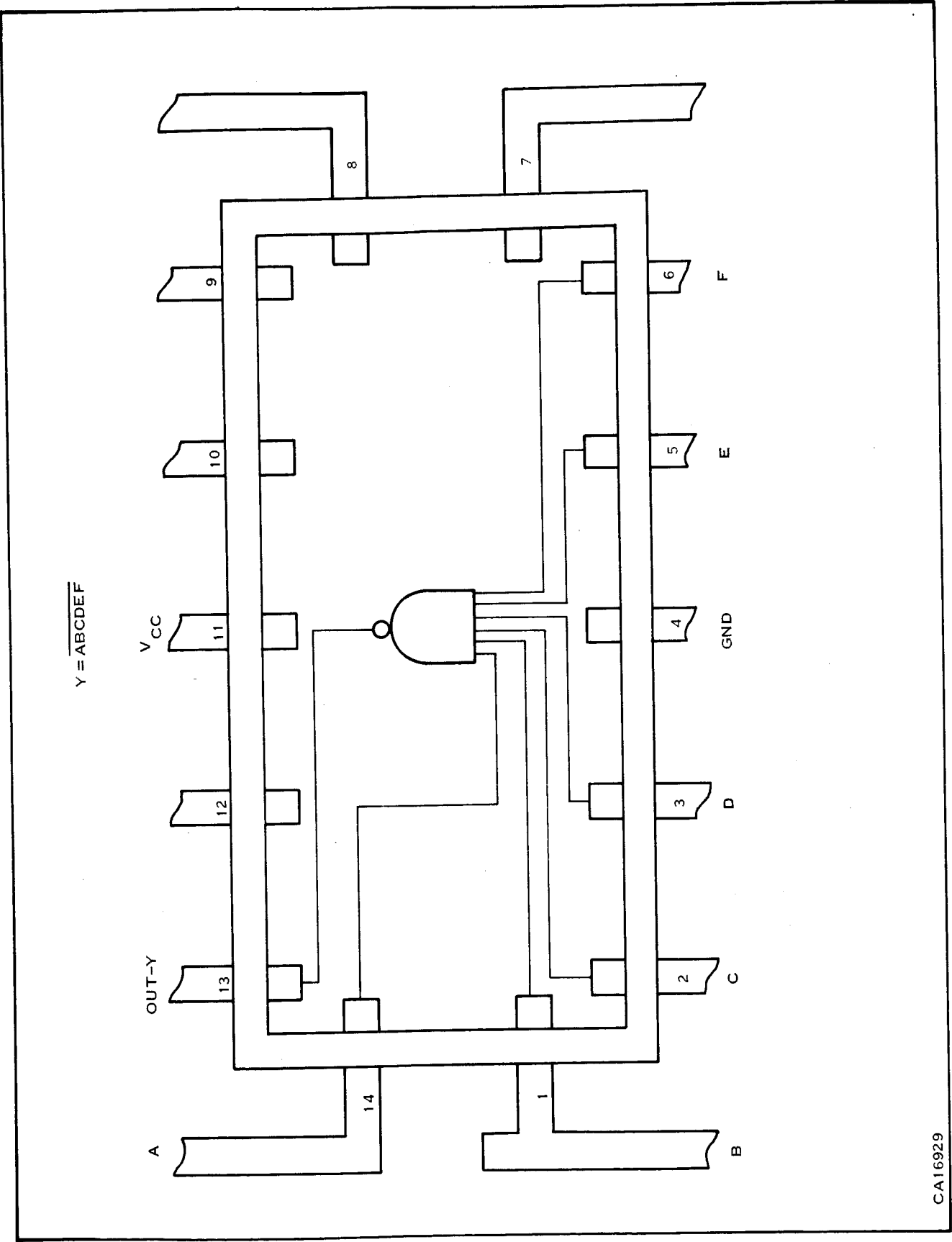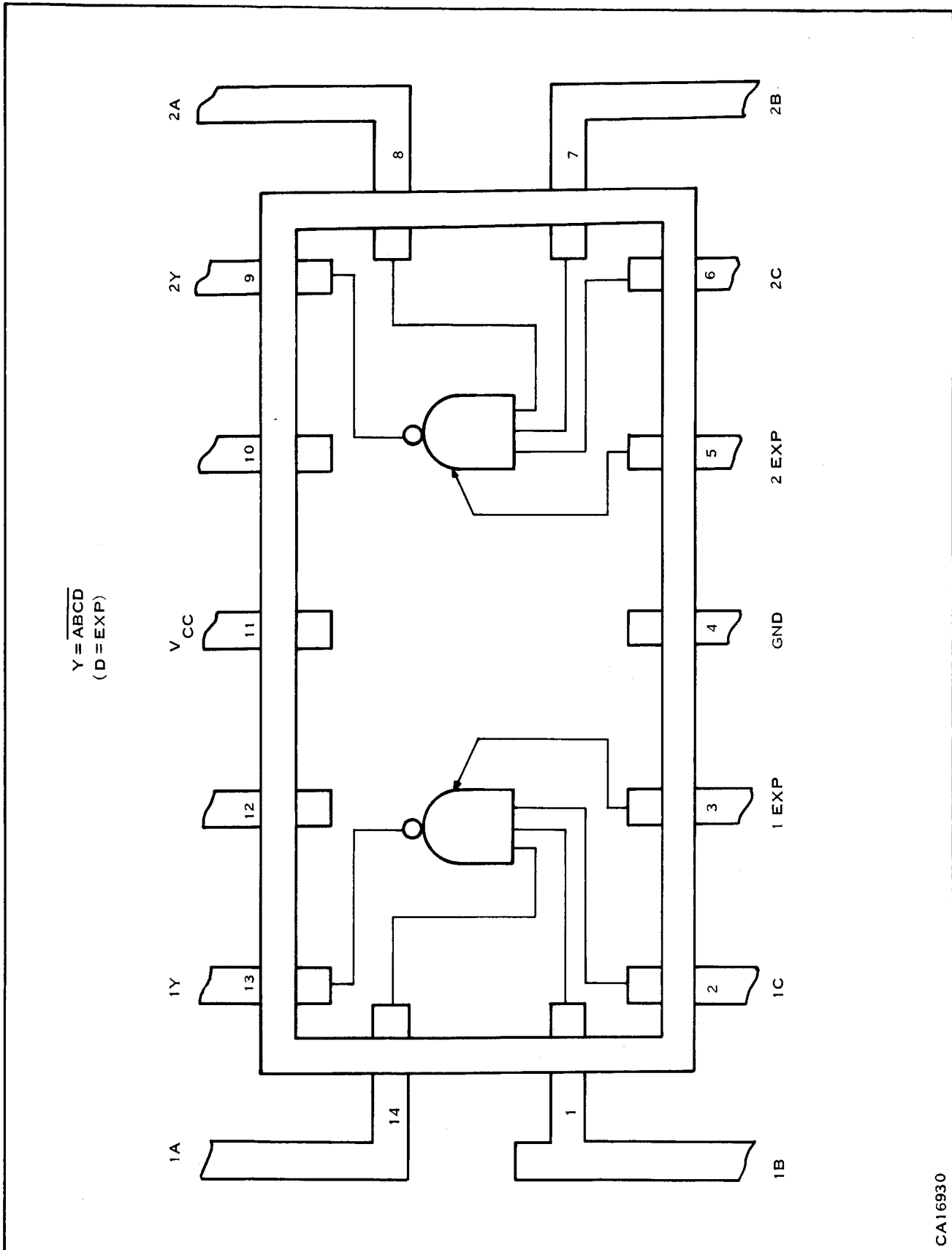
Figure 35.   Dual-3 NAND Gate Bonding Diagram (Top View)

CA16930
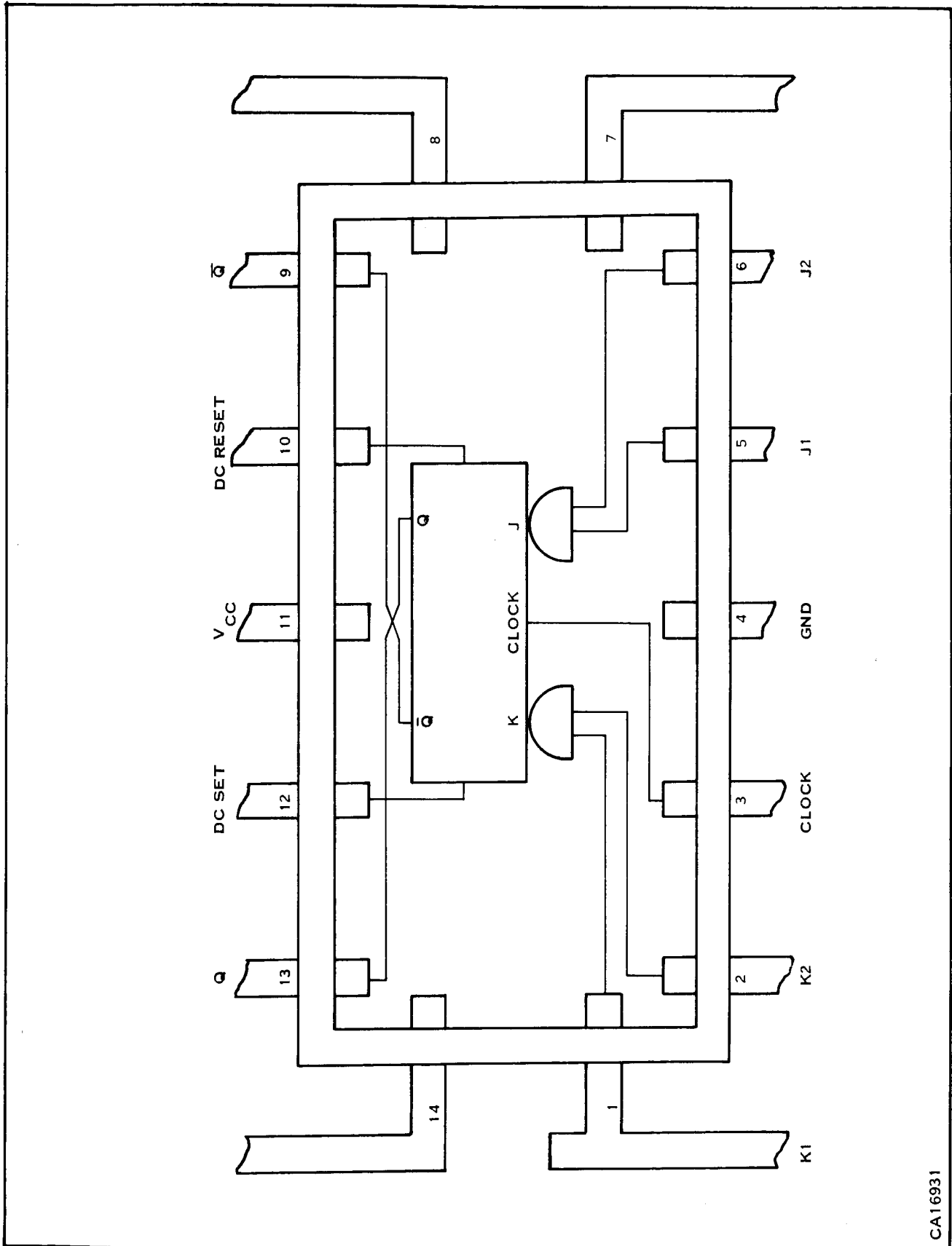
Figure 36. J-K Flip-Flop Bonding Diagram (Top View)

CA16931
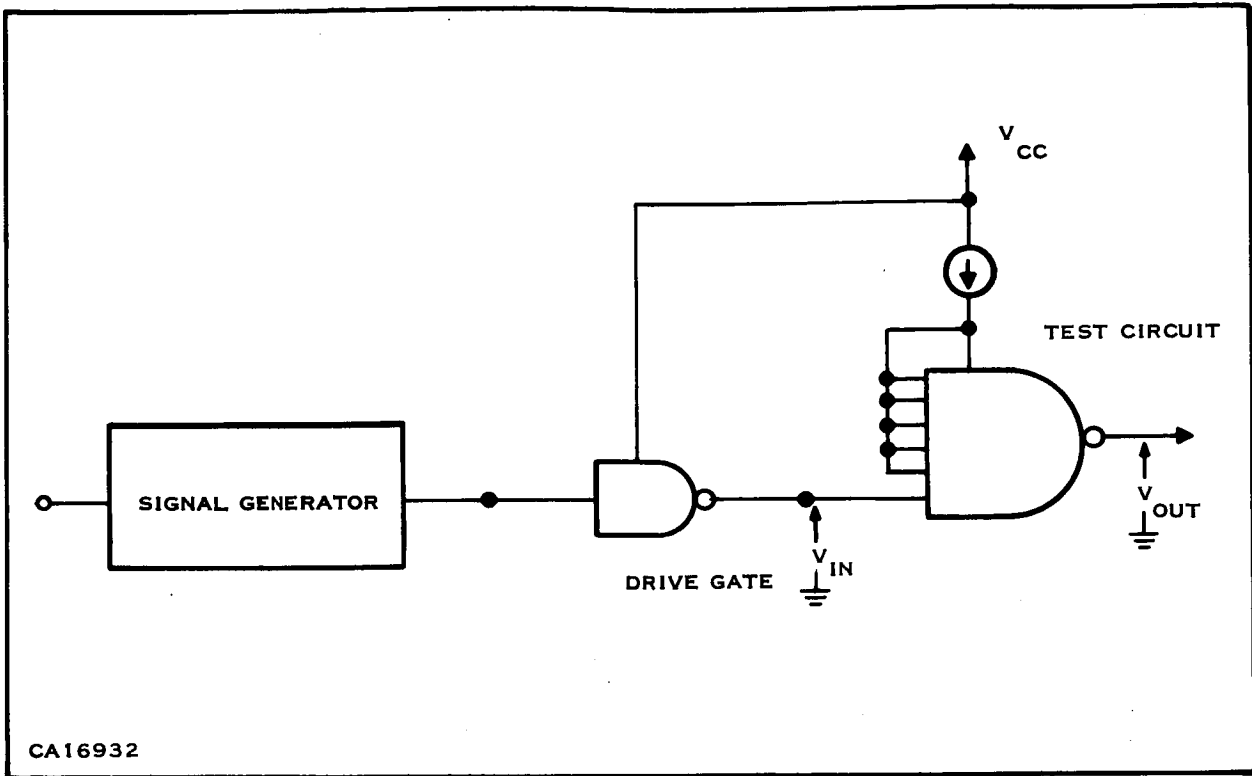
Figure 37. Characterization Setup

$$t_p = \frac{t_{d0} + t_{d1}}{2}$$
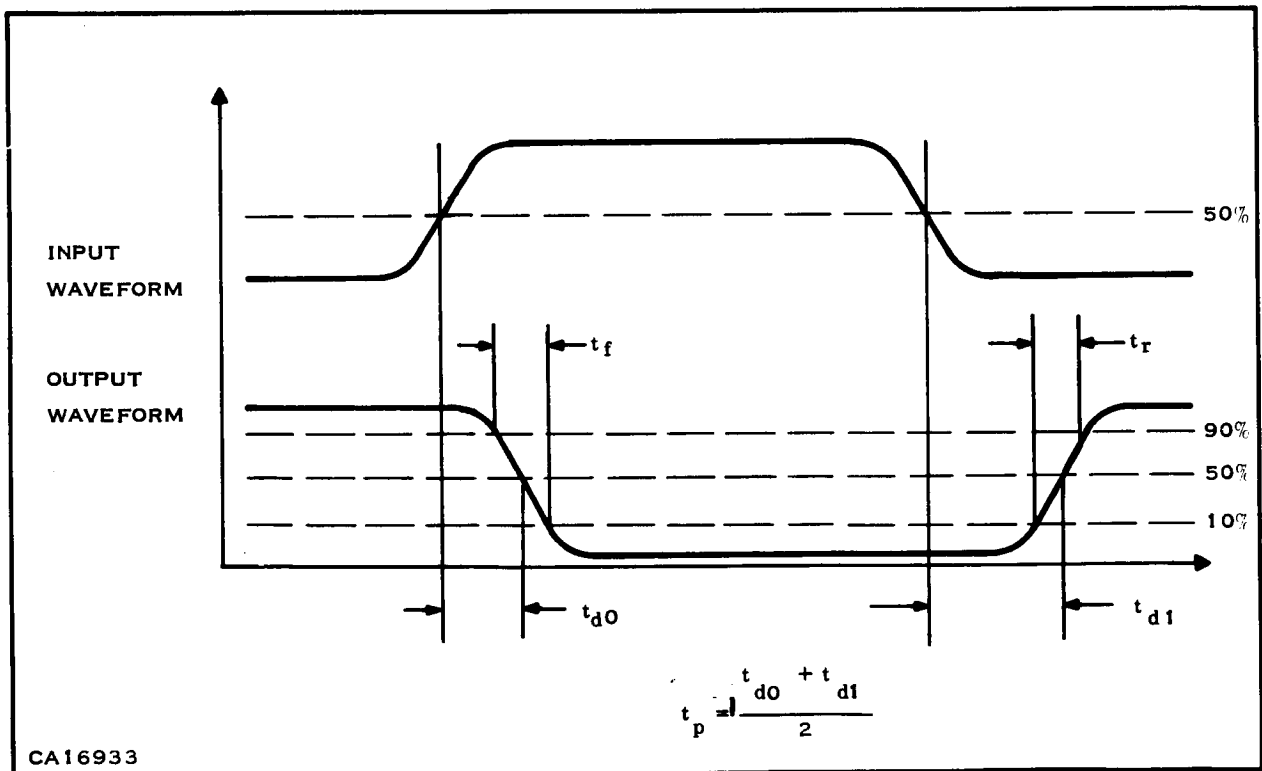
Figure 38. Definition of Switching Times (Gates)

Rise time (t_r) refers to the time it takes the output voltage to rise from 10 to the 90 percent points. Fall time (t_f) is defined in a similar manner, as indicated in the same figure.

The data from two circuits will be presented here. The first gate (MS-4) was fabricated in lot MF-AB and is typical of the NAND gates fabricated during this contract. The second gate (MS-71) was fabricated in lot MF-AG, which had low h_{FE} on the output transistors. The major effect of the low h_{FE} will be in transient performance and in noise immunity.

Titles of figures showing performance for both gates are listed here for convenient reference and followed by comments on the performance.

Figure 39—Standby Power versus V_{CC} (MS-4)
Figure 40—Standby Power versus V_{CC} (MS-71)
Figure 41—Frequency versus Power (MS-4)
Figure 42—Frequency versus Power (MS-71)
Figure 43—Power versus Temperature (MS-4)
Figure 44—Power versus Temperature (MS-71)
Figure 45—Switching Waveforms—t_{d0}, Gate (MS-4)
Figure 46—Switching Waveforms—t_{d1}, Gate (MS-4)
Figure 47—Switching Waveform—t_{d0}, Gate (MS-71)
Figure 48—Switching Waveform—t_{d1}, Gate (MS-71)
Figure 49—Propagation Delay versus Power (MS-4, MS-71)
Figure 50—Switching Times versus Temperature (MS-4)
Figure 51—Switching Times versus Temperature (MS-71)
Figure 52—F_{max} versus Power (MS-4, MS-71)
Figure 53—F_{max} versus C_{LOAD} (MS-4, MS-71)
Figure 54—V_{OUT} versus V_{IN} (MS-4)
Figure 55—V_{OUT} versus V_{IN} (MS-71)
Figure 56—Worst-Case V_{OUT} versus V_{IN} (MS-4)
Figure 57—Worst-Case V_{OUT} versus V_{IN} (MS-71)
Figure 58—V_{OUT} versus I_{SOURCE} (MS-4)
Figure 59—V_{OUT} versus I_{SOURCE} (MS-71)
Figure 60—V_{OUT} versus I_{SINK} (MS-4)
Figure 61—V_{OUT} versus I_{SINK} (MS-71)
Figure 62—V_{IN} versus I_{IN} (MS-4)
Figure 63—V_{IN} versus I_{IN} (MS-71)
Figure 64—AC Noise (MS-4, MS-71)
Figure 65—Trigger Level versus Temperature (MS-4)
Figure 66—Trigger Level versus Temperature (MS-71)
Figure 67—Propagation Delay versus Emitters to V_{CC} (MS-4, MS-71)
Figure 68—Current Due to Emitters at V_{CC} (MS-4)
Figure 69—Current Due to Emitters at V_{CC} (MS-71)
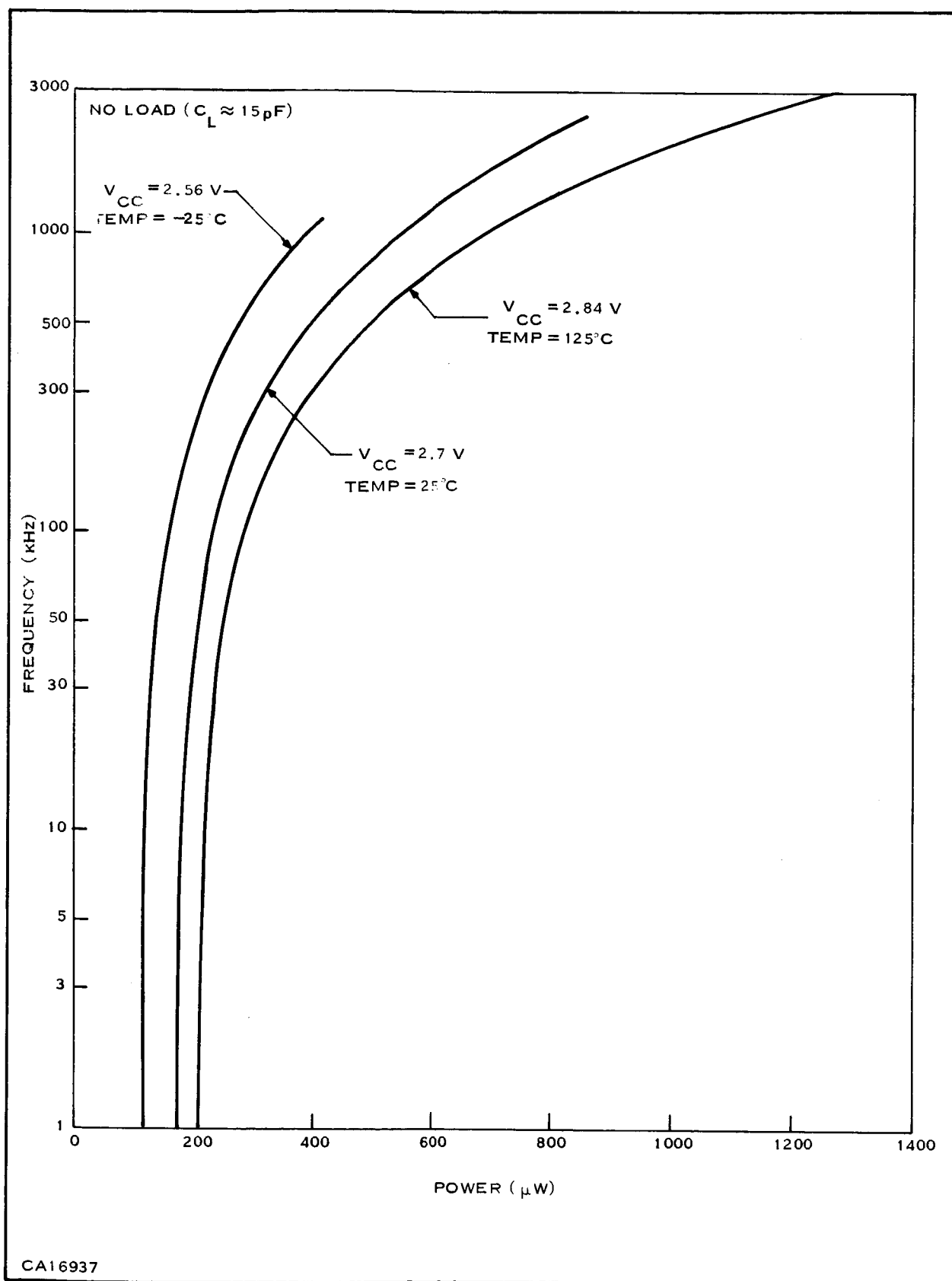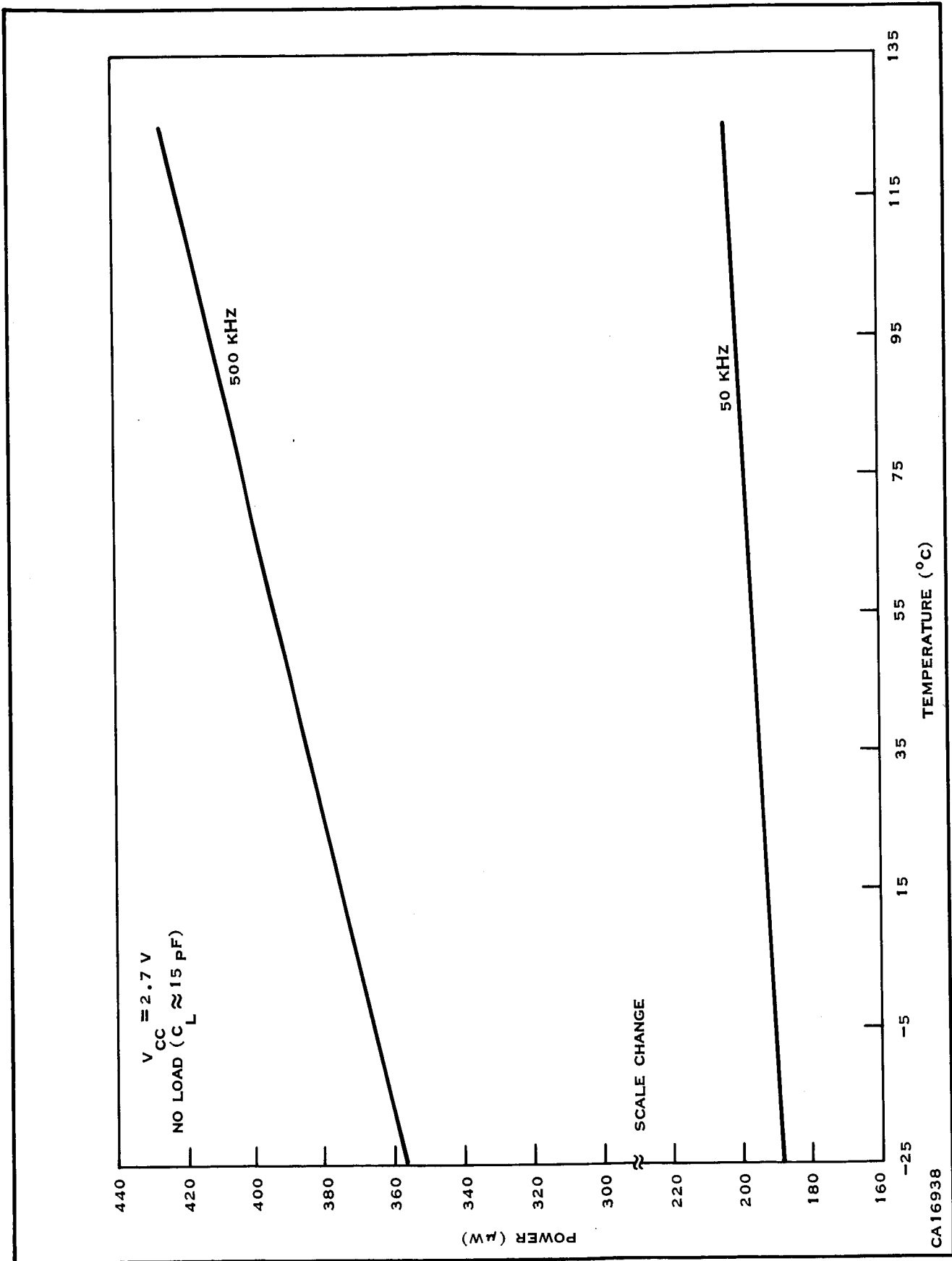
Figure 39. Standby Power versus V_{CC} (MS-4)

Figure 40.   Standby Power versus V_{CC} (MS-71)

NO LOAD ($C_L \approx 15$ pF)

V_{CC} =2.56 V
TEMP= –25°C

V_{CC} =2.84 V
TEMP =125°C

V_{CC} =2.7 V
TEMP =25°C

FREQUENCY (kHz)

POWER (μW)

CA16935

Figure 41.   Frequency versus Power (MS-4)

Figure 42. Frequency versus Power (MS-71)

Figure 43.   Power versus Temperature (MS-4)

CA16938

Figure 44. Power versus Temperature (MS-71)

CA16939

(a.) NO LOAD
20 ns/DIV
-25°C
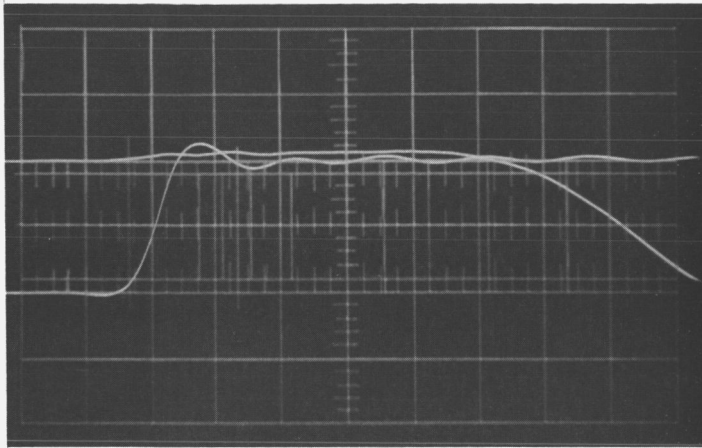
(b.) FLIP-FLOP LOAD
50 ns/DIV
-25°C
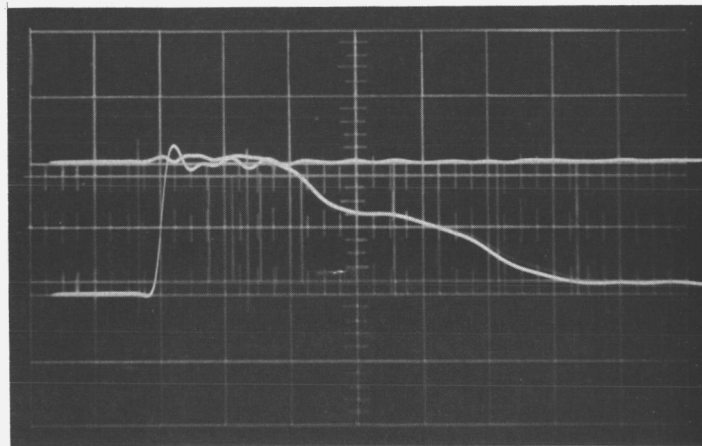
(c.) NAND LOAD
20 ns/DIV
-25°C
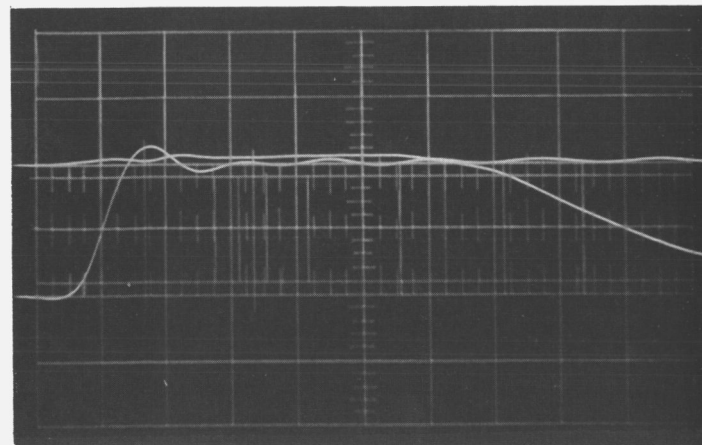
CA16940(1-3)

Figure 45.   Switching Waveforms — t_{d0}, Gate (MS-4)
(Sheet 1 of 3)

(d.) NO LOAD
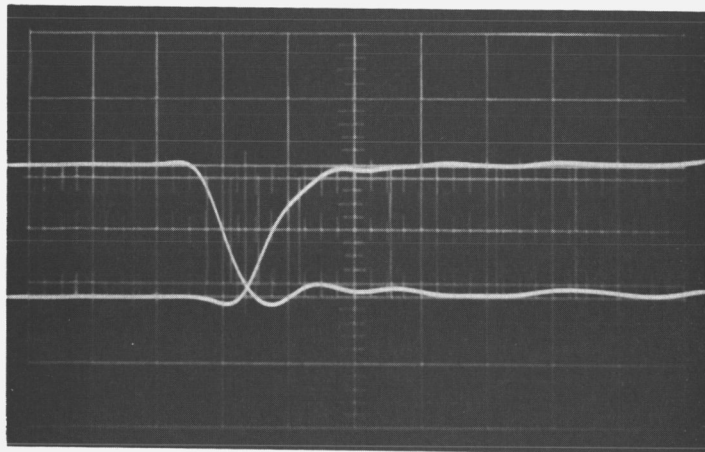20 ns/DIV
25°C
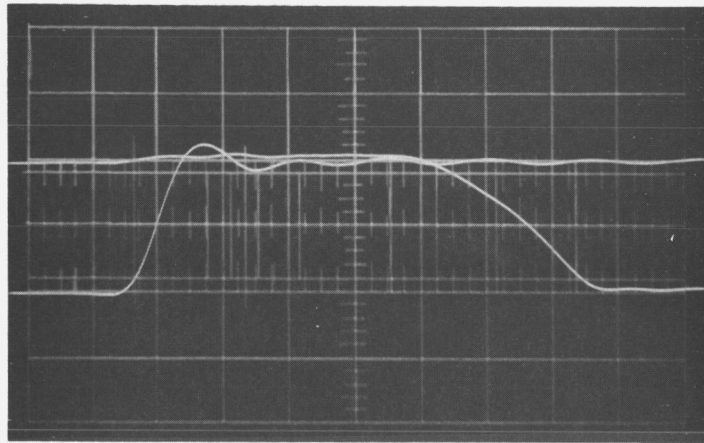
(e.) FLIP-FLOP LOAD
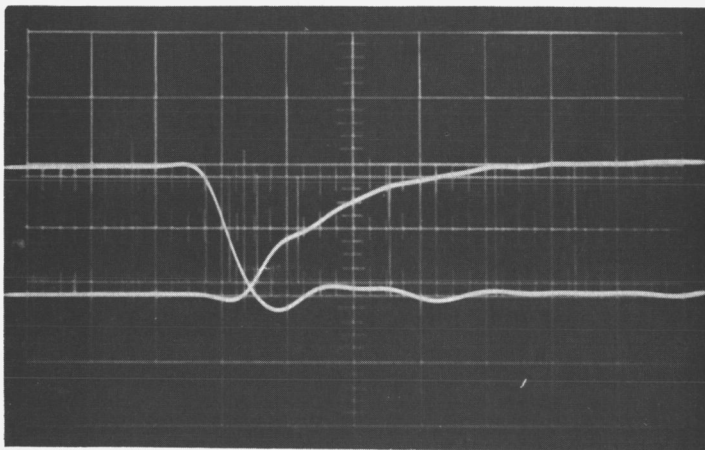20 ns/DIV
25°C
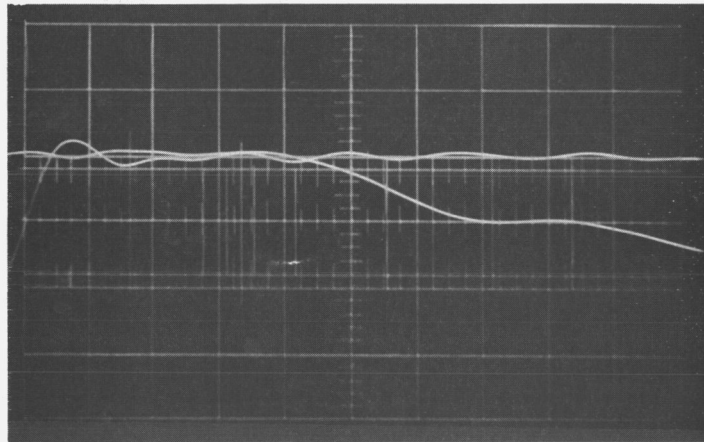
(f.) NAND LOAD
20 ns/DIV
25°C
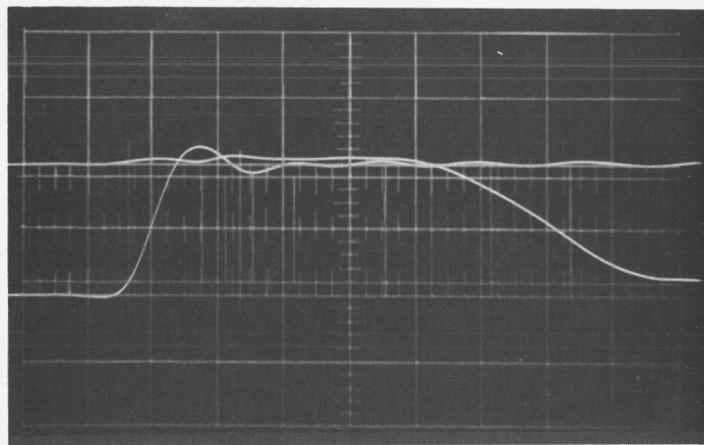
CA16940(2-3)

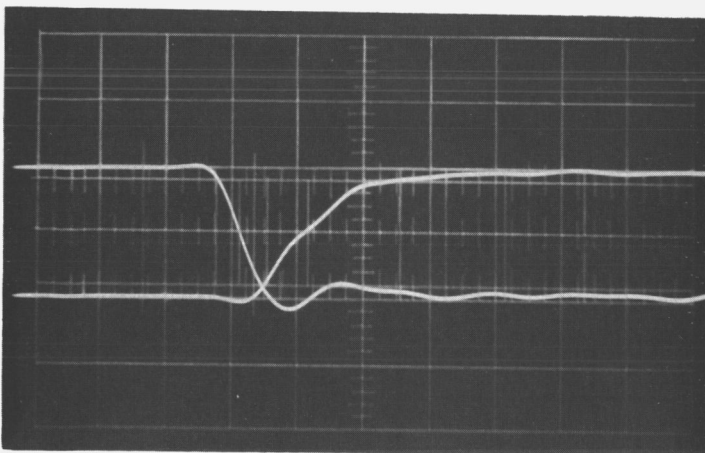Figure 45.   Switching Waveforms — t_{d0}, Gate (MS-4)
(Sheet 2 of 3)

(g.) NO LOAD
20 ns/DIV
125°C
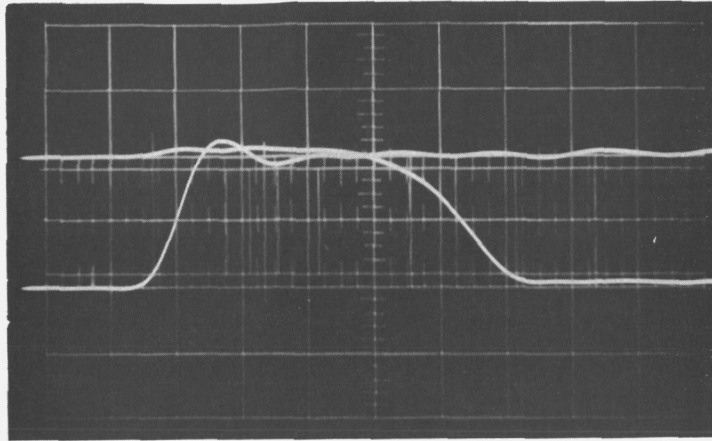
(h.) FLIP-FLOP LOAD
20 ns/DIV
125°C
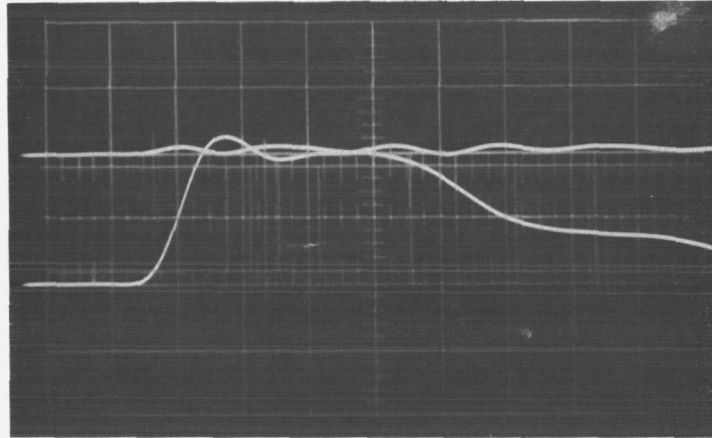
(i.) NAND LOAD
20 ns/DIV
125°C
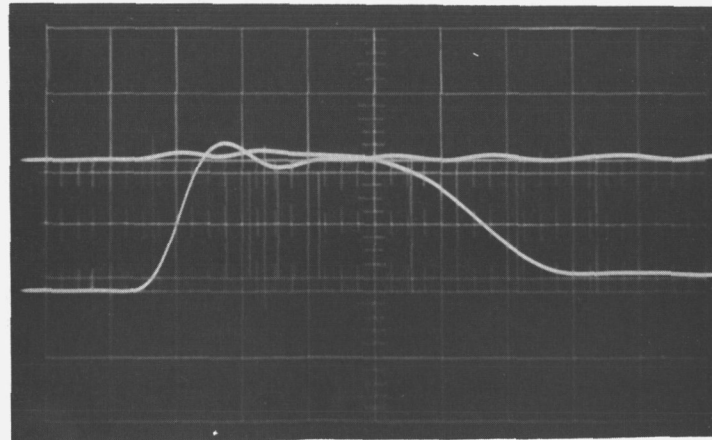
CA16940(3-3)

Figure 45. Switching Waveforms — t_{d0}, Gate (MS-4)
(Sheet 3 of 3)

(a.) NO LOAD
20 ns/DIV
-25°C
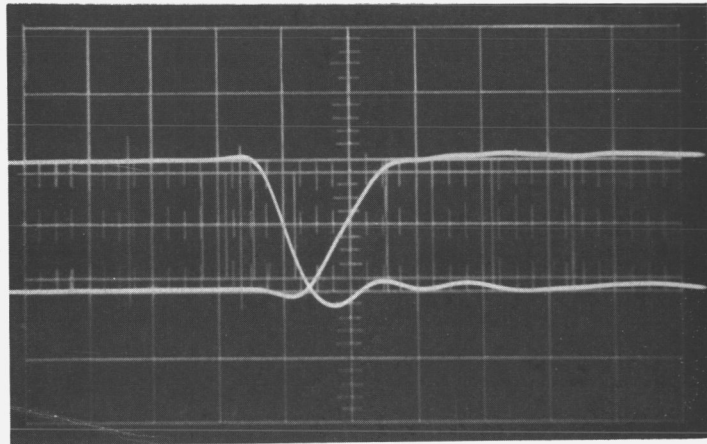
(b.) FLIP-FLOP LOAD
20 ns/DIV
-25°C
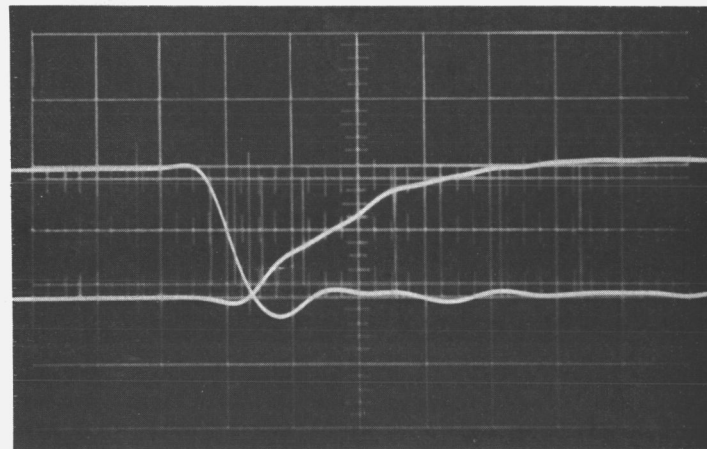
(c.) NAND LOAD
20 ns/DIV
-25°C
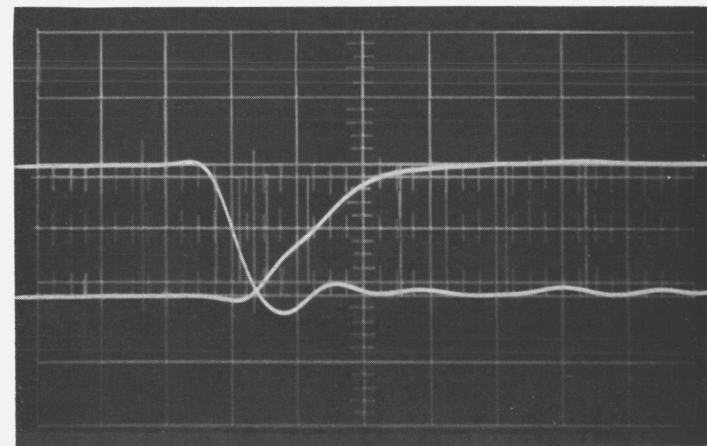
CA16941(1-3)

Figure 46.   Switching Waveforms – t_{d1}, Gate (MS-4)
(Sheet 1 of 3)

(d.) NO LOAD
20 ns/DIV
25°C
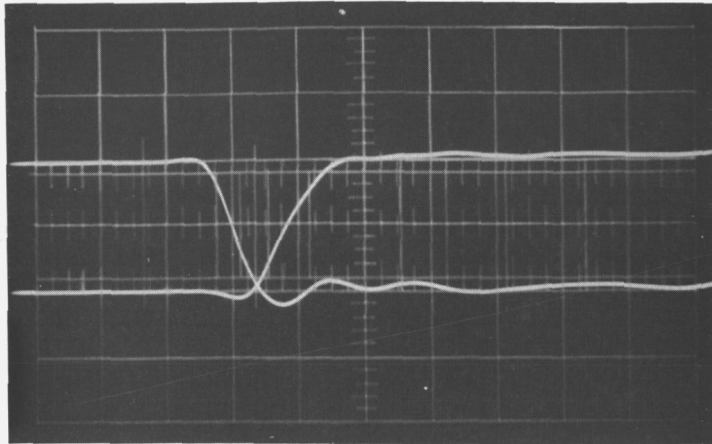
(e.) FLIP-FLOP LOAD
20 ns/DIV
25°C
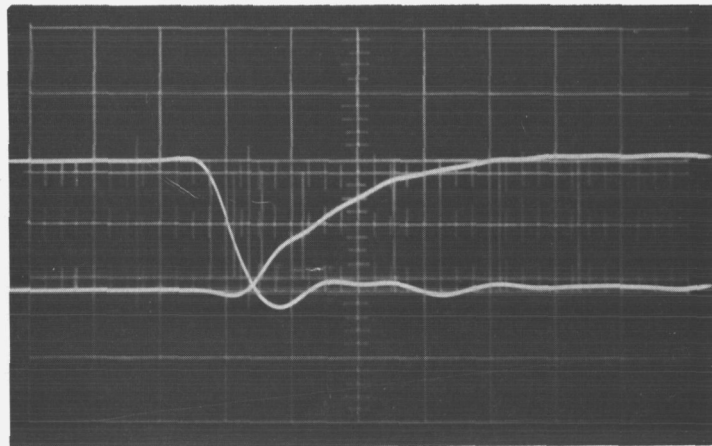
(f.) NAND LOAD
20 ns/DIV
25°C
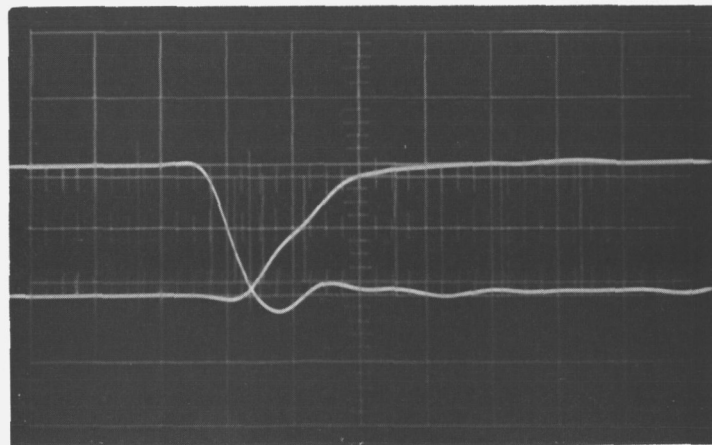
CA16941(2-3)

Figure 46.   Switching Waveforms — t_{d1}, Gate (MS-4)
(Sheet 2 of 3)

(g.) NO LOAD
20 ns/DIV
125°C
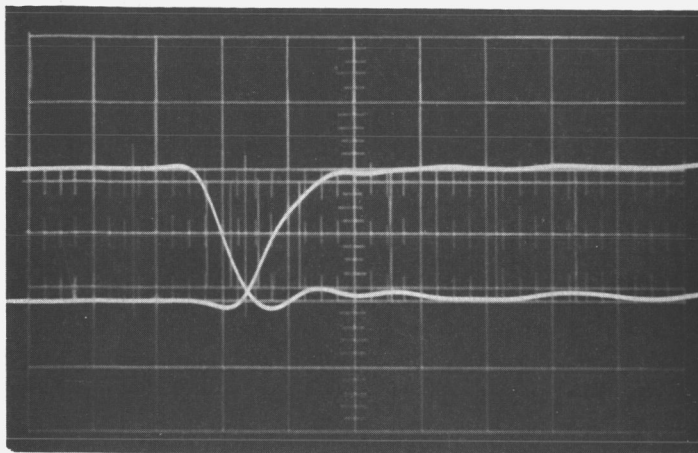
(h.) FLIP-FLOP LOAD
20 ns/DIV
125°C
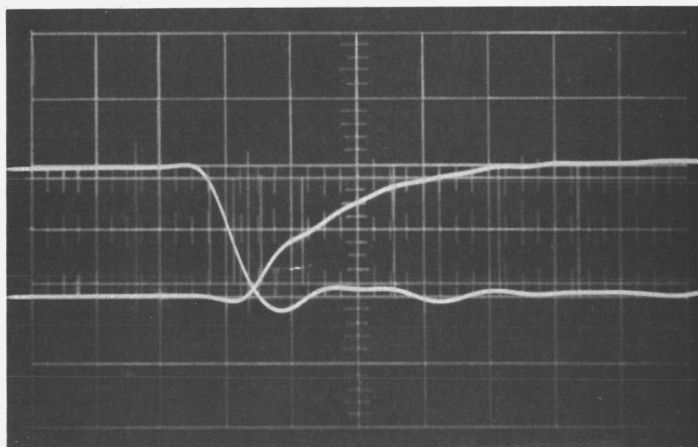
(i.) NAND LOAD
20 ns/DIV
125°C
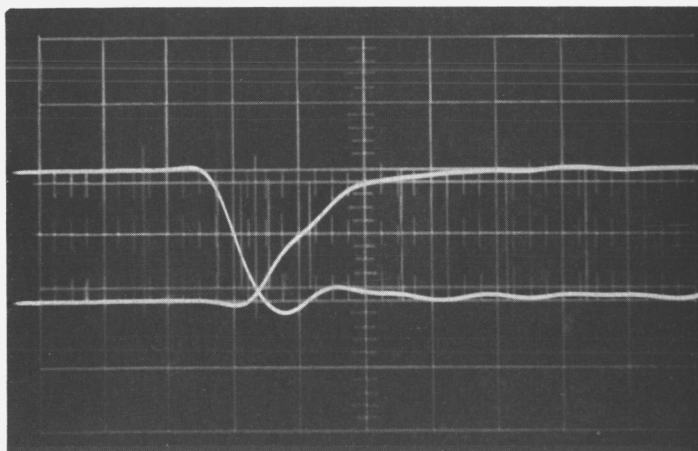
CA16941(3-3)

Figure 46.   Switching Waveforms − t_{d1}, Gate (MS-4)
(Sheet 3 of 3)

71

(a.) NO LOAD
20 ns/DIV
-25°C

(b.) FLIP-FLOP LOAD
50 ns/DIV
-25°C

(c.) NAND LOAD
50 ns/DIV
-25°C
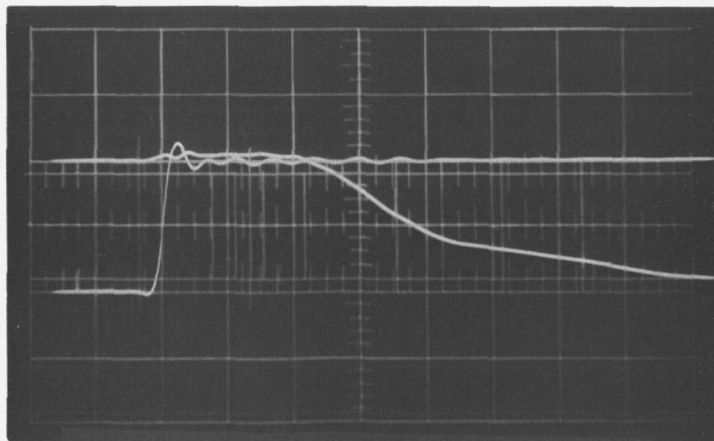
CA16942(1-3)

Figure 47.   Switching Waveforms — t_{d0}, Gate (MS-71)
(Sheet 1 of 3)

(d.) NO LOAD
20 ns/DIV
25°C
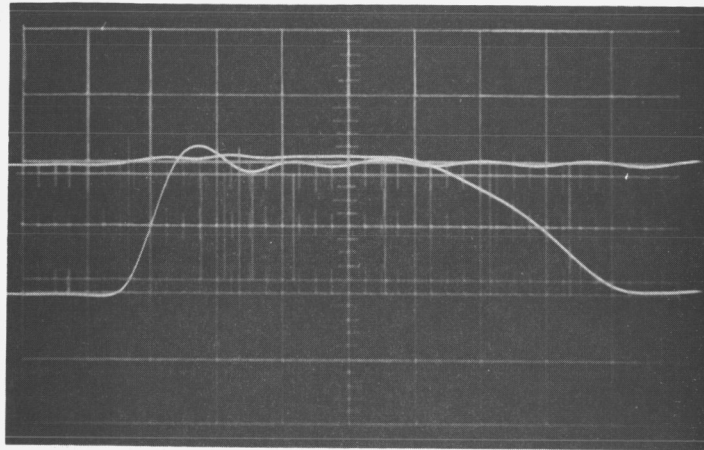
(e.) FLIP-FLOP LOAD
20 ns/DIV
25°C
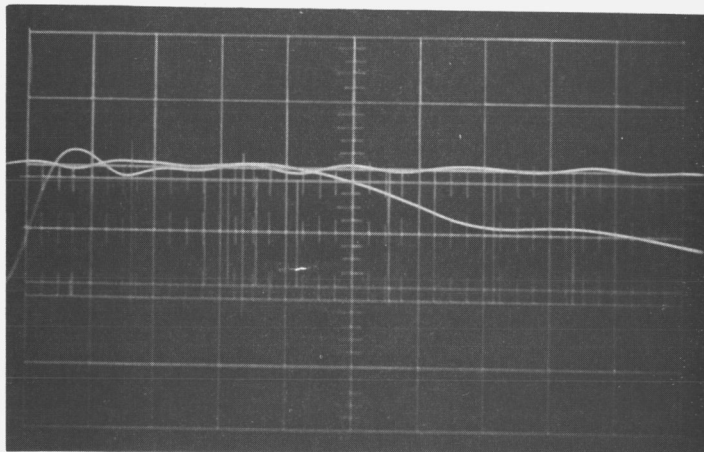
(f.) NAND LOAD
20 ns/DIV
25°C
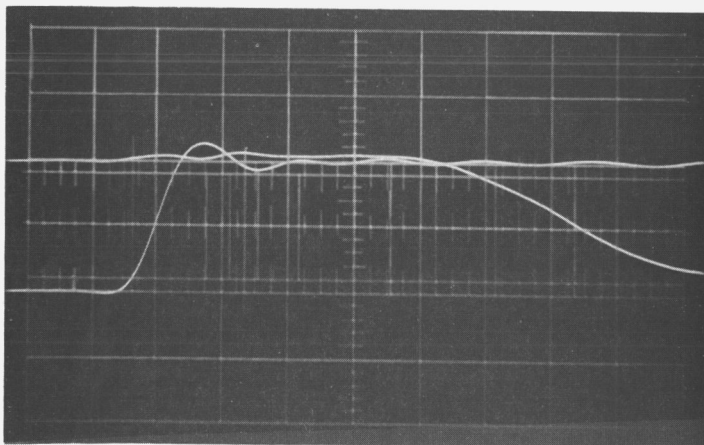
CA16942(2-3)

Figure 47. Switching Waveforms – t_{d0}, Gate (MS-71)
(Sheet 2 of 3)

(g.) NO LOAD
20 ns/DIV
125°C
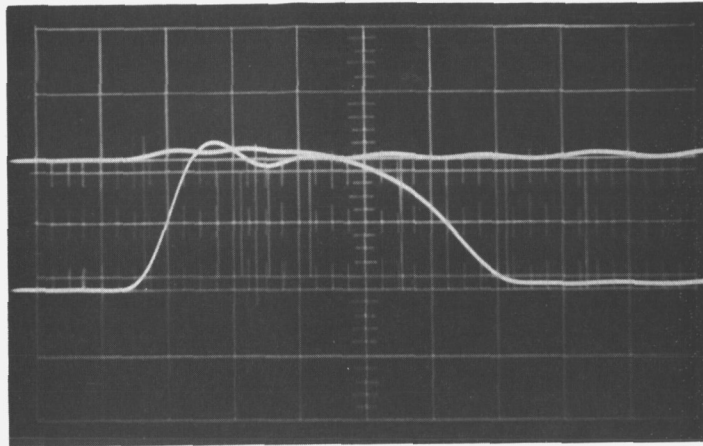
(h.) FLIP-FLOP LOAD
20 ns/DIV
125°C
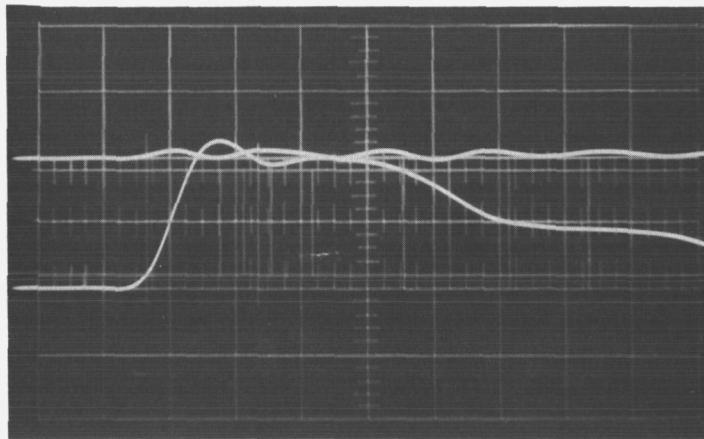
(i.) NAND LOAD
20 ns/DIV
125°C
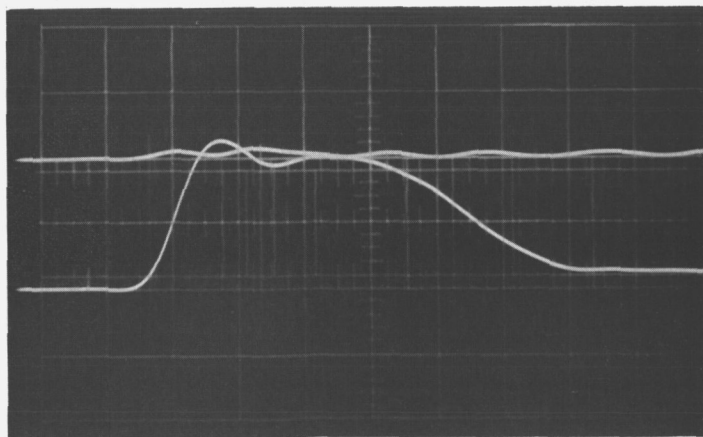
CA16942(3-3)

Figure 47. Switching Waveforms – t_{d0}, Gate (MS-71)
(Sheet 3 of 3)

(a.) NO LOAD
20 ns/DIV
-25°C
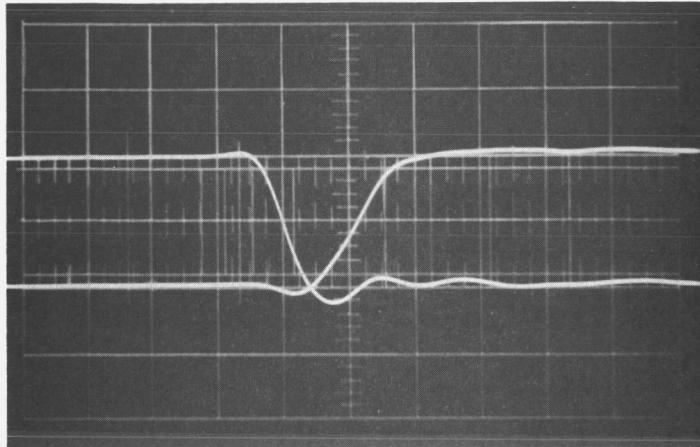
(b.) FLIP-FLOP LOAD
20 ns/DIV
-25°C
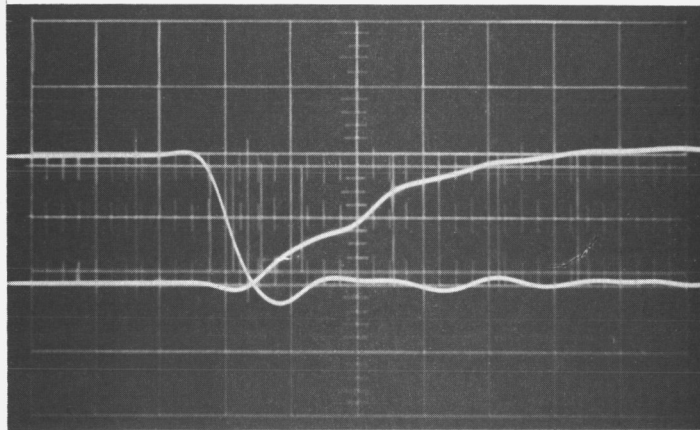
(c.) NAND LOAD
20 ns/DIV
-25°C
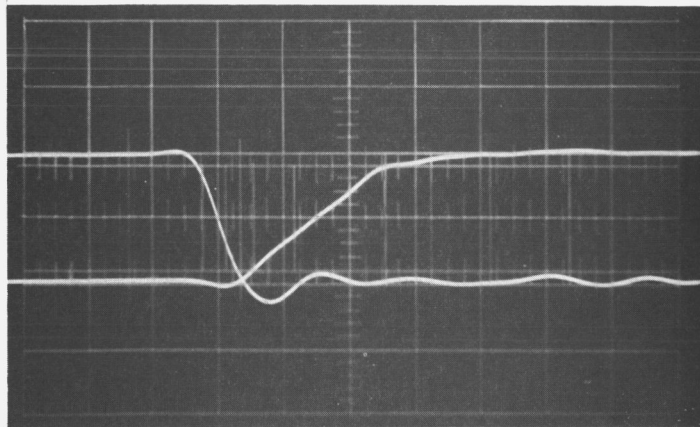
CA16943(1-3)

Figure 48. Switching Waveforms – t_{d1}, Gate (MS-71)
(Sheet 1 of 3)

(d.) NO LOAD
20 ns/DIV
25°C
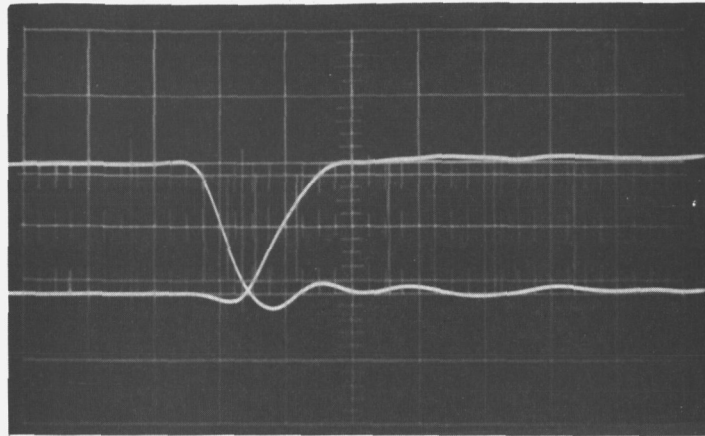
(e.) FLIP-FLOP LOAD
20 ns/DIV
25°C
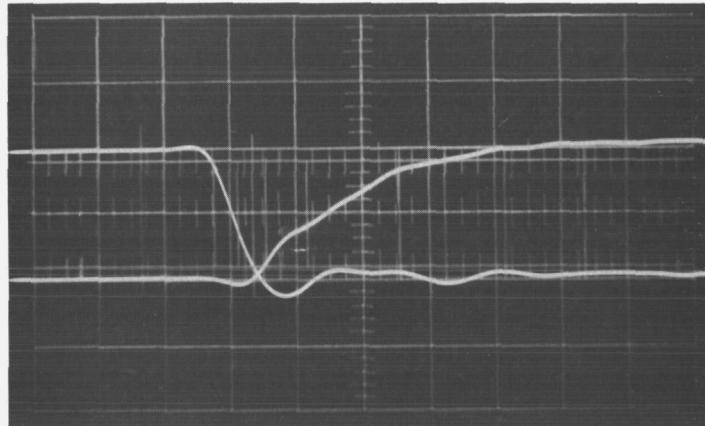
(f.) NAND LOAD
20 ns/DIV
25°C
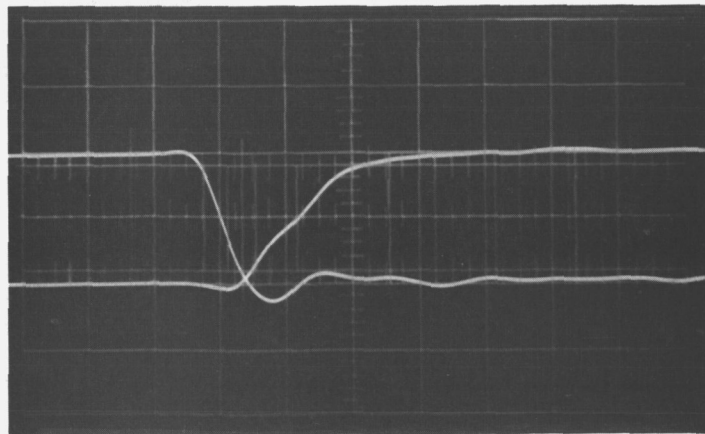
CA16943(2-3)

Figure 48.   Switching Waveforms – t_{d1}, Gate (MS-71)
(Sheet 2 of 3)

(g.) NO LOAD
20 ns/DIV
125°C

(h.) FLIP-FLOP LOAD
20 ns/DIV
125°C

(i.) NAND LOAD
20 ns/DIV
125°C

CA16943(3-3)

Figure 48. Switching Waveforms $- t_{d1}$, Gate (MS-71)
(Sheet 3 of 3)
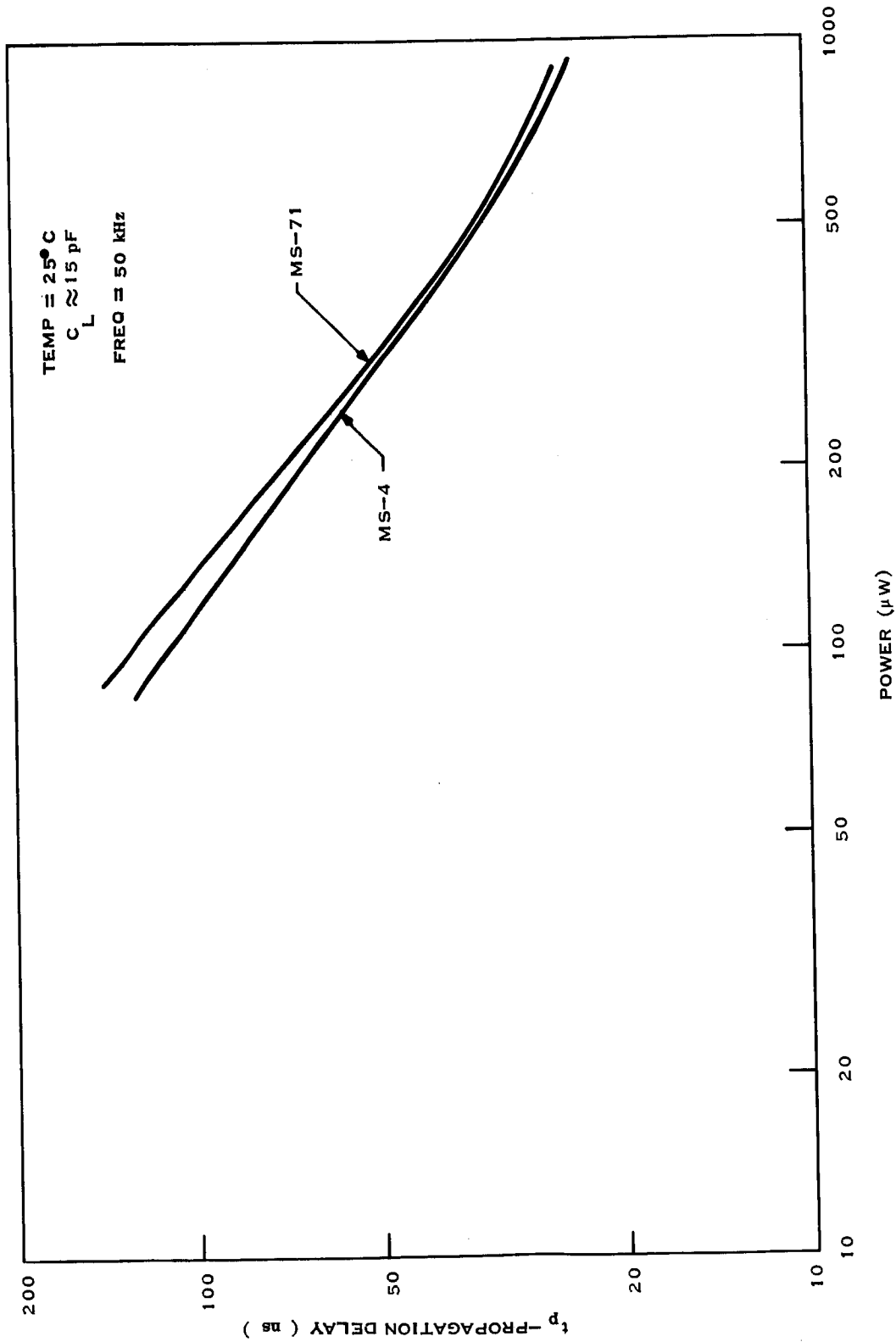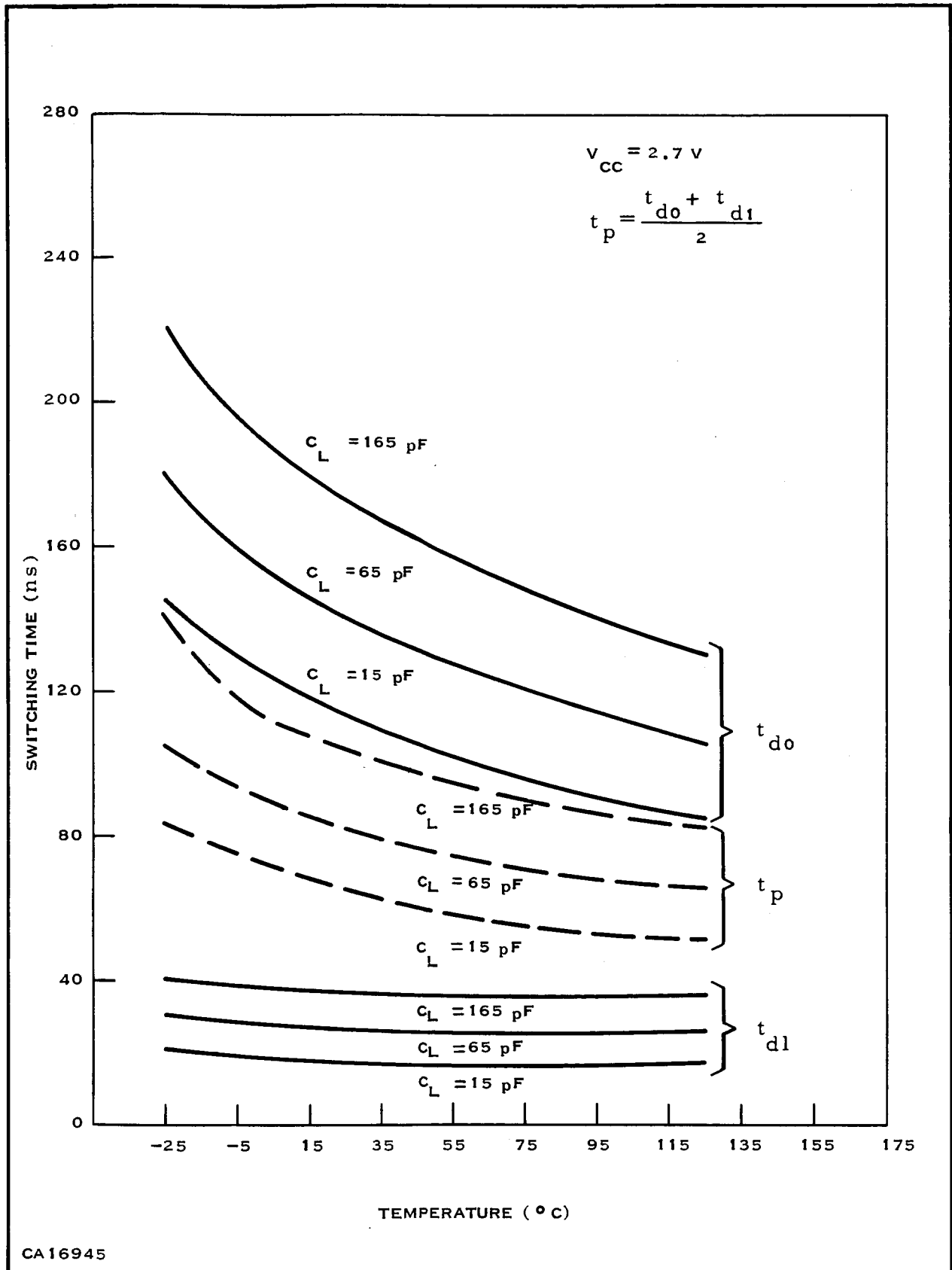
Figure 49. Propagation Delay versus Power (MS-4, MS-71)

CA16944

$$V_{cc} = 2.7 \text{ v}$$

$$t_p = \frac{t_{do} + t_{d1}}{2}$$

Figure 50. Switching Times versus Temperature (MS-4)

CA 16945
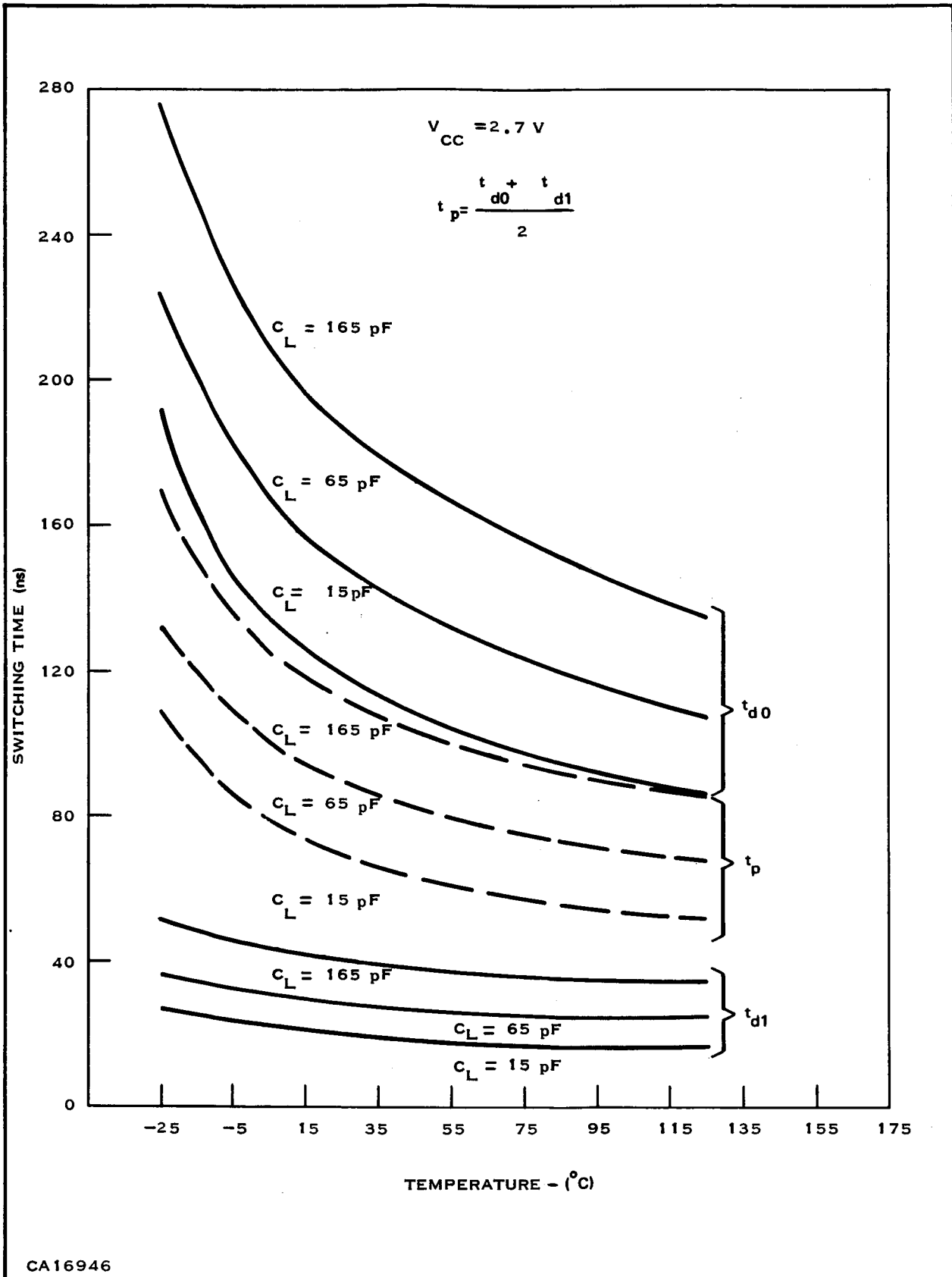
Figure 51. Switching Times versus Temperature (MS–71)
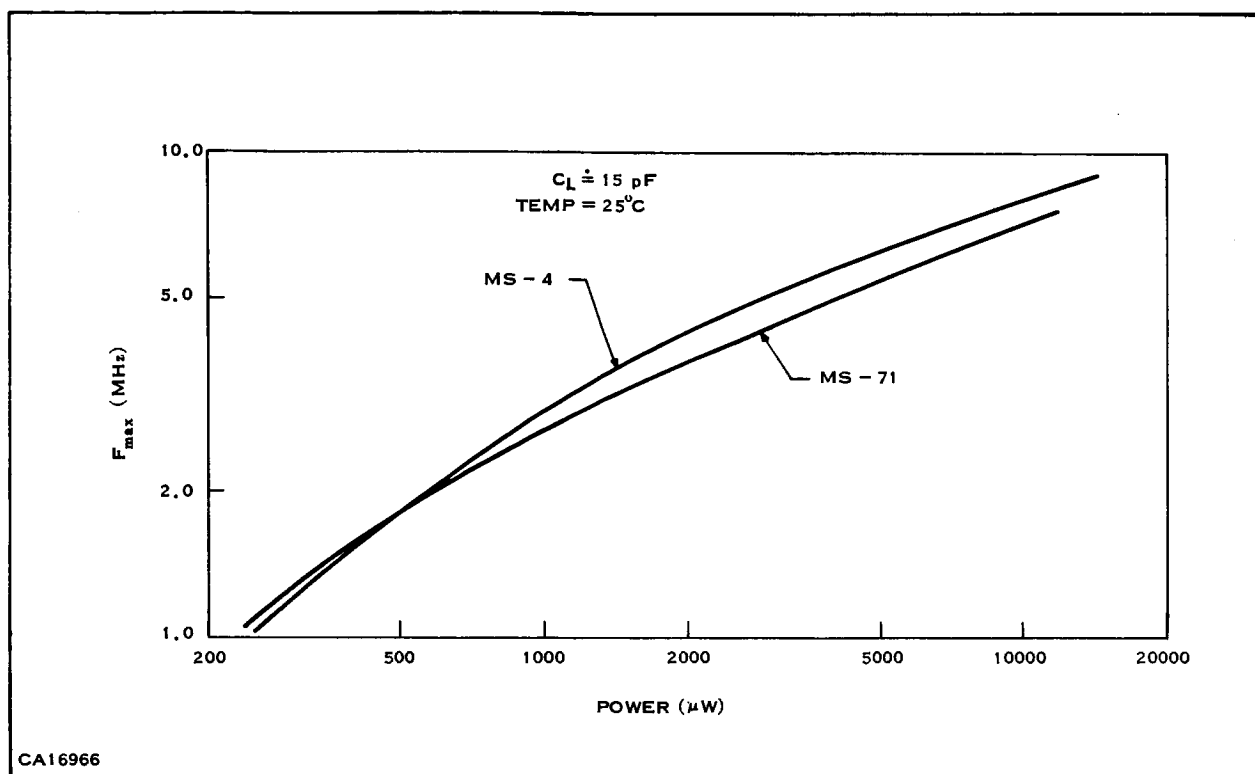
Figure 52. F_{max} versus Power (MS-4, MS-71)

These tests were conducted using the NAND gate as an inverter. One emitter of the input transistor was used as the input; the other 5 emitters were tied to V_{CC}. This condition will give worst-case power due to emitter-to-emitter current gain.

The data presented in Figures 39 through 69 is self-explanatory, but a few comments will be made to point out special features. The standby power plots of Figures 39 and 40 were made by varying V_{CC} from 2.0 V to 5.0 V. The "0" standby power was within the 300 μW specification at 2.7 V. Since these circuits are relatively independent of V_{CC}, they are capable of operating over a large supply voltage range. This makes them compatible with standard digital circuits, for example—Texas Instruments Series 54L.

The frequency plots of Figures 41 and 42 show that under some conditions the 2-MHz operating frequency was not met. The basic problem here is not in the complementary inverter section but in the T^2L input. The circuit speed is really dictated by the amount of parasitic capacitance associated with the multi-emitter input transistor (Q3 of Figure 2) and the f_t of this device. With dielectric isolation, for example, it would be theorized that 10-MHz operation at these power levels could be obtained (see Figure 6.) Even though the circuits' maximum operating frequency was somewhat low compared to the 2 MHz contract specification, these circuits had twice the operating frequency of the circuit fabricated during Contract NAS1-4350.

The unique effect that the TCR of the diffused resistor has is shown in Figures 43 and 44. The worst-case power is approximately 25°C for low frequencies. At higher frequencies, the power due to switching transients is predominant.
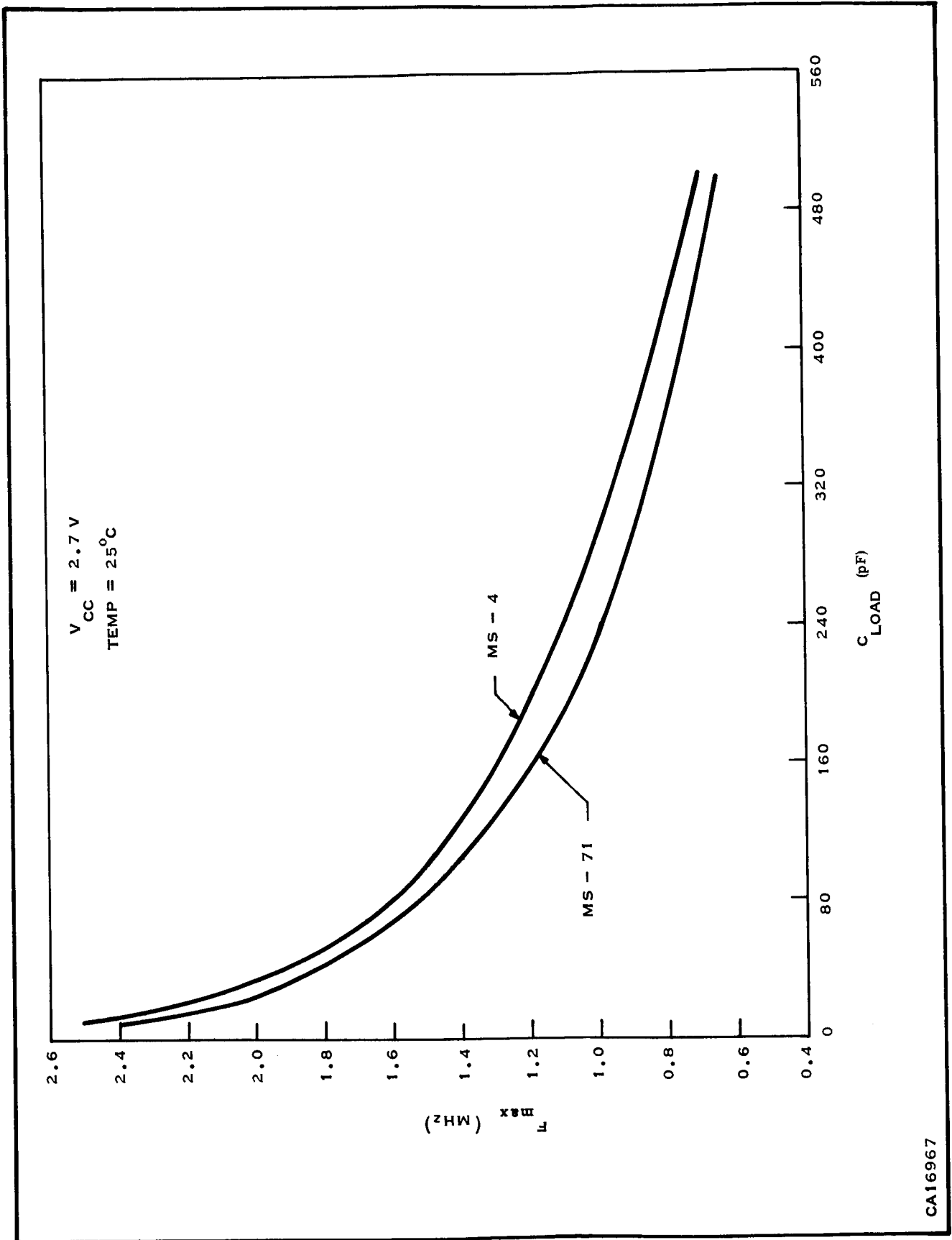
Figure 53. F_{max} versus C_{LOAD} (MS-4, MS-71)

CA16967
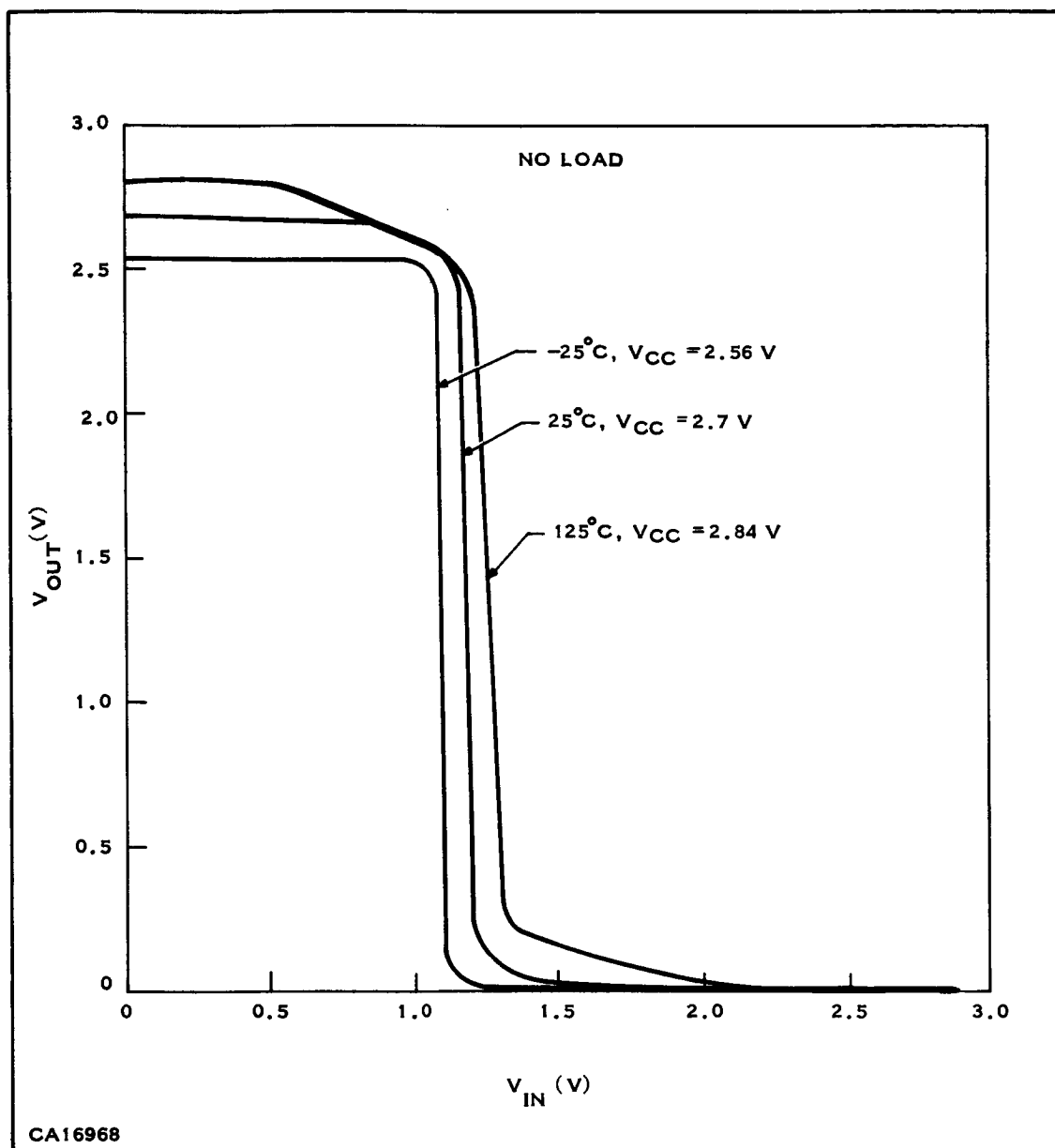
Figure 54. V_{OUT} versus V_{IN} (MS-4)

Switching waveforms of Figures 45 through 48 completely describe the gates' switching performance. The major portion of propagation delay is contributed by t_{d0}. Notice that gate MS-71 has longer fall times due to the low h_{FE} of the output transistors.

The speed-power plot of Figure 49 was obtained by varying V_{CC} from 2 to 5 V. The power-speed product at 2.7 V is approximately 14 picojoules for both gates. The test frequency was 50 KHz.

Switching times over the temperature range are shown in Figures 50 and 51. The curves are plotted for capacitance loads of 15, 65 and 165 pF.
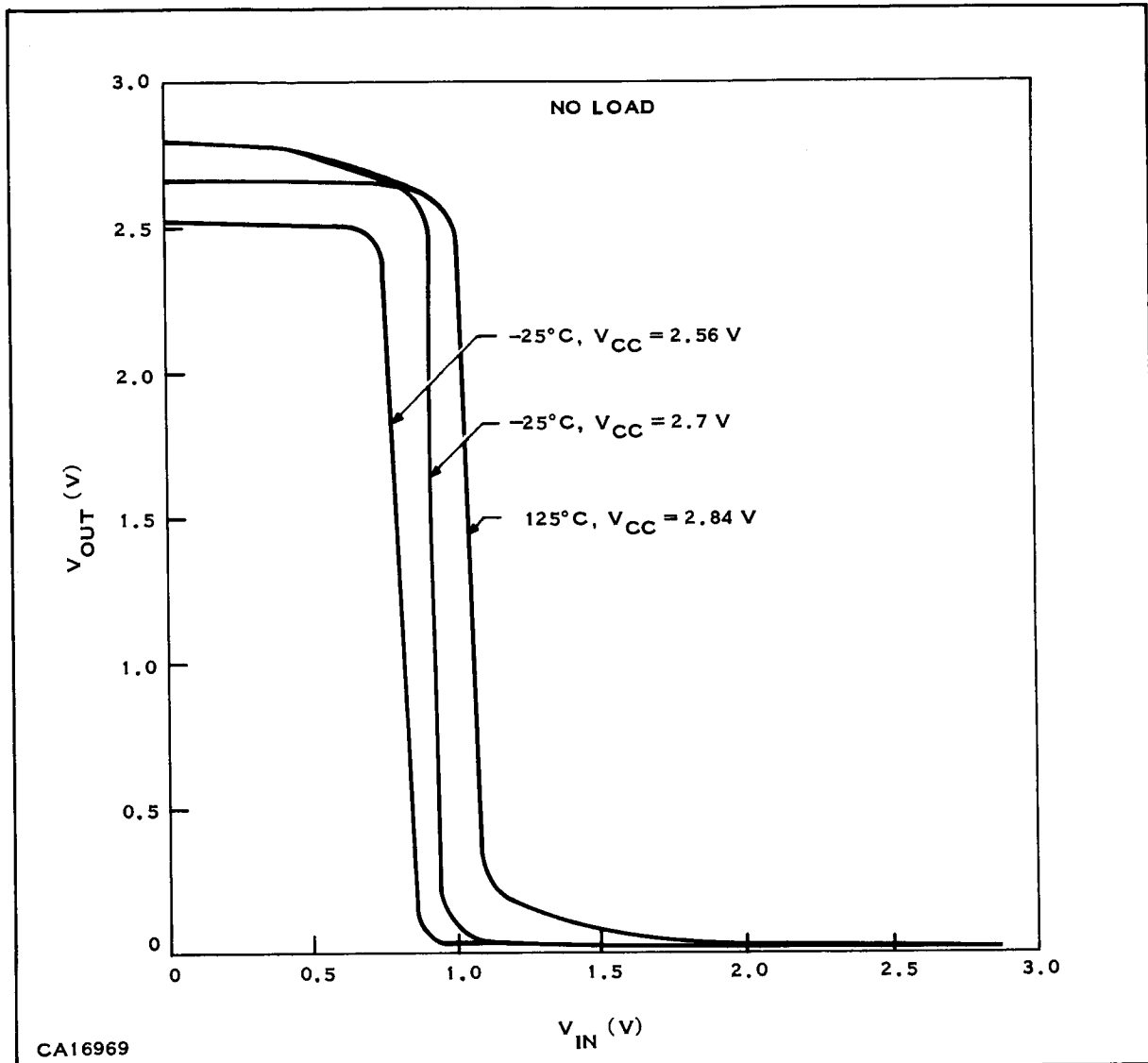
Figure 55. V_{OUT} versus V_{IN} (MS-71)

The maximum operating frequency (F_{max}) plot of Figure 52 was obtained by varying V_{CC} from 2.0 to 6.0 V. The power is the power at F_{max}. The effect of load capacitance is shown in Figure 53.

Voltage transfer curves of Figures 54 and 55 were taken at NO LOAD condition. The worst-case plots of Figures 56 and 57 were obtained by varying the worst-case voltage, temperature, and loading conditions required by the contract. The data given on the plots were calculated using the method explained by Lynn et al.[3] The following definitions apply:

V_ℓ—logic swing

NM^0—noise margin for a logical "0" input

The figure contains the following annotations:

$V_f = 2.4 \text{ V}$

TRANSITION WIDTH=0.5 V

$NM^0 = 0.95 \text{ V}$

$NS^0 = 1.0 \text{ V}$

$NM^1 = 1.0 \text{ V}$

$NS^1 = 1.2 \text{ V}$

$$NI^0 = \frac{NS^0}{V_f} = \frac{1.0}{2.4} = 0.42$$

$$NI^1 = \frac{NS^1}{V_f} = \frac{1.2}{2.4} = 0.50$$

LOGICAL "1" OPERATING POINT

UNITY GAIN POINT

LOGICAL "0" OPERATING POINT

UNITY GAIN POINT

CA16970
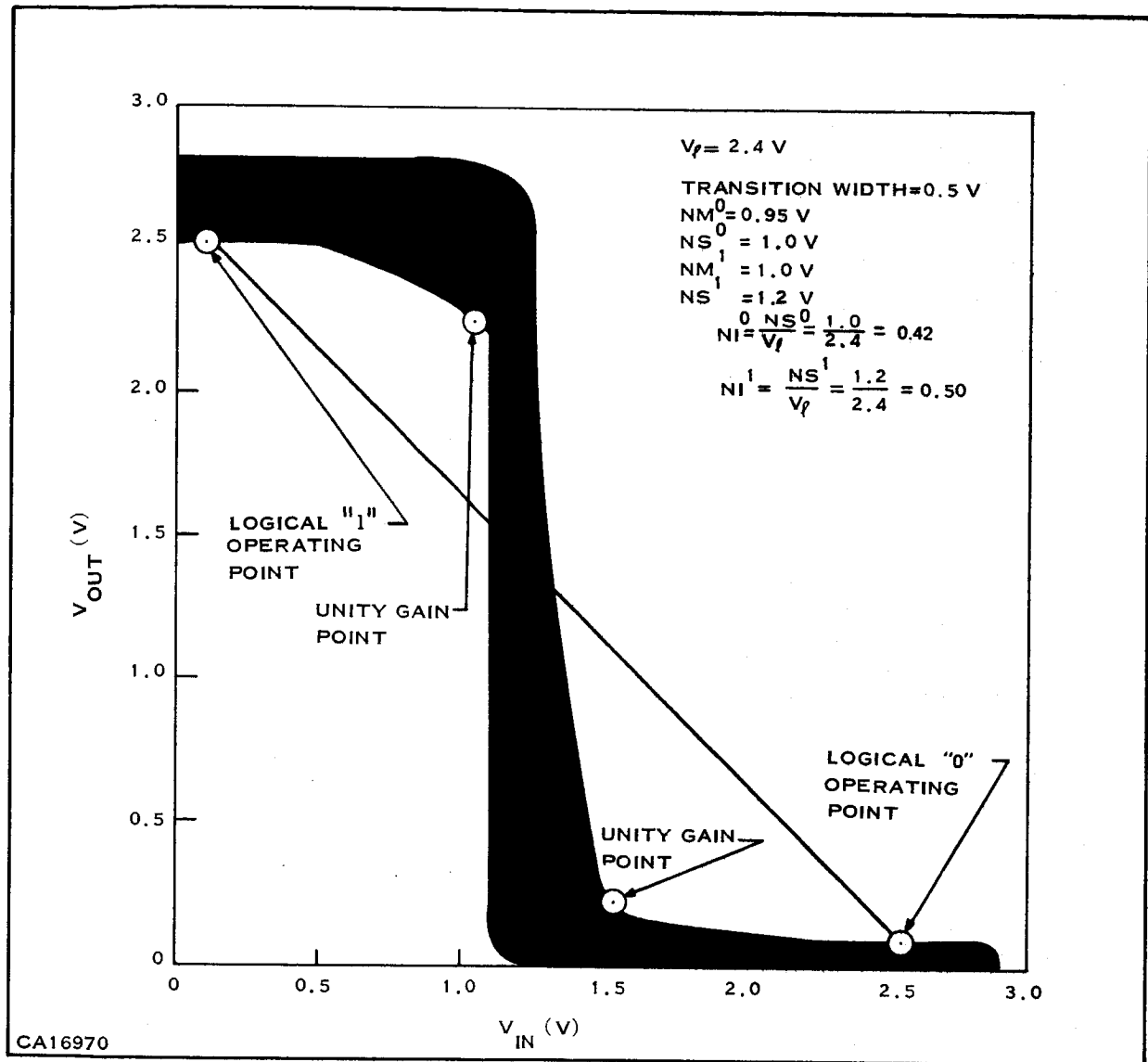
Figure 56. Worst-Case V_{OUT} versus V_{IN} (MS-4)

NM^1—noise margin for a logical "1" input

NS^0—noise sensitivity for a logical "0" input

NS^1—noise sensitivity for a logical "1" input

NI—ratio of noise sensitivity to logic swing (NS/V_ϱ).

In Figure 57, the low h_{FE} of the output transistors causes a wide transition width. These plots also point out one of the salient features of complementary output digital logic. Both the "1" and "0" operating levels are clamped at $V_{CC} - V_{CE(sat)}$ and $V_{CE(sat)}$ of the transistors. The nominal value for both the PNP and NPN transistor of $V_{CE(sat)}$ is less than 0.1 V.

The figure contains the following labels and annotations:

$V_\ell = 2.325\ V$

TRANSITION WIDTH = 1.25 V

$NM^0 = 0.55\ V$

$NS^0 = 0.595\ V$

$NM^1 = 0.525$

$NS^1 = 0.925$

$NI^0 = \dfrac{NS^0}{V_\ell} = \dfrac{0.575}{2.325} = 0.25$

$NI^1 = \dfrac{NS^1}{V_\ell} = \dfrac{0.925}{2.325} = 0.40$

LOGICAL "1" OPERATING POINT

UNITY GAIN POINT

UNITY GAIN POINT

LOGICAL "0" OPERATING POINT

V_{OUT} (V)

V_{IN} (V)

CA16971
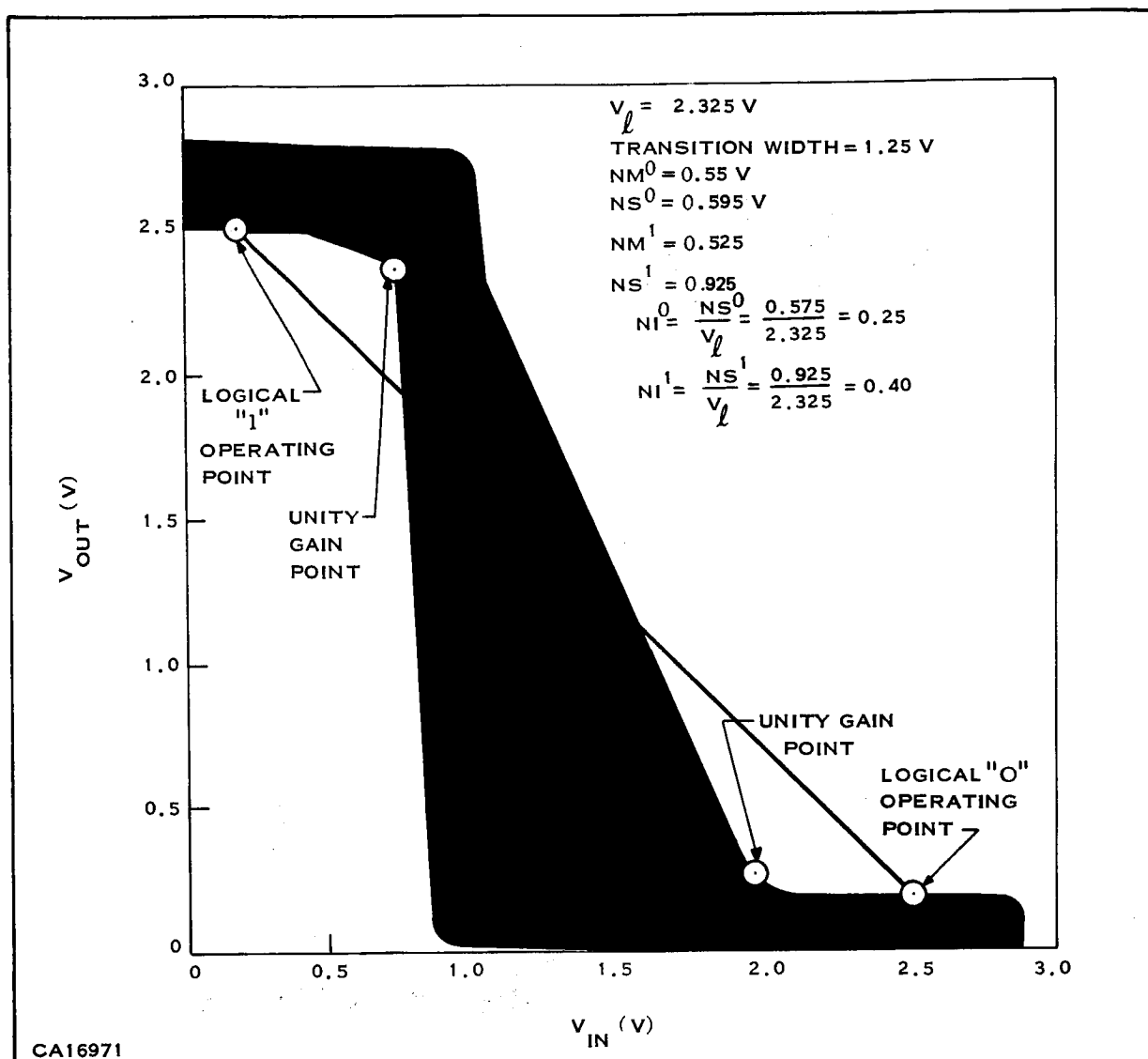
Figure 57. Worst-Case V_{OUT} versus V_{IN} (MS-71)

Plots of Figures 58 through 61 show that the output impedance in both the "1" and "0" operating levels is the $R_{(sat)}$ of the PNP and NPN transistor until the transistors are pulled out of saturation. The output impedance is less than 200 Ω while the transistors are in saturation.

Input impedance can be obtained from Figures 62 and 63. The input impedance is approximately 25 kΩ. Also, the value predicted by Equation (6) for a fan-out of 5 is 455 μA while the curve gives approximately 400 μA at -25°C.

The ac noise plot of Figure 64 points out another feature of the complementary output; that is, any ac noise will be suppressed since the output will always be an ON transistor.
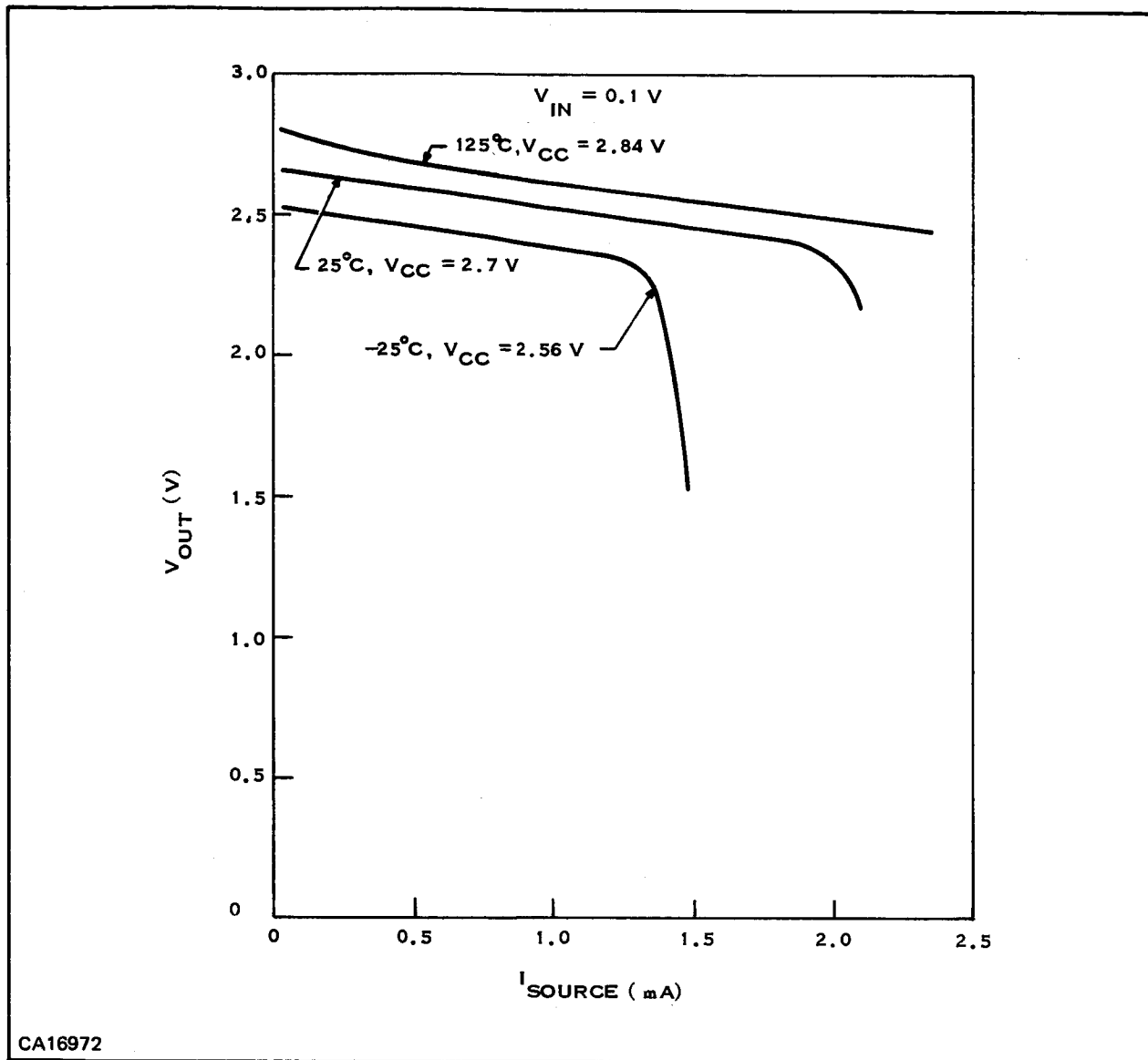
Figure 58. V_{OUT} versus I_{SOURCE} (MS-4)

The trigger level plots of Figures 65 and 66 were taken with the following definitions:

"0" Trigger Level—when every portion of the output waveform is within 0.2 V of the final value.

"1" Trigger Level—when any portion of the output waveform goes above 0.2 V of the initial value.

Figure 67 shows the adverse effect that the 5 unused emitters to V_{CC} have on propagation delay. These emitters add capacitance that the input transistor must charge and discharge.

When the unused 5 emitters of the gating transistor are returned to V_{CC} and the input is at ground, then there is a wasted current flowing equal to $5\beta_I I_{BQ3}$, where β_I is the emitter-to-emitter
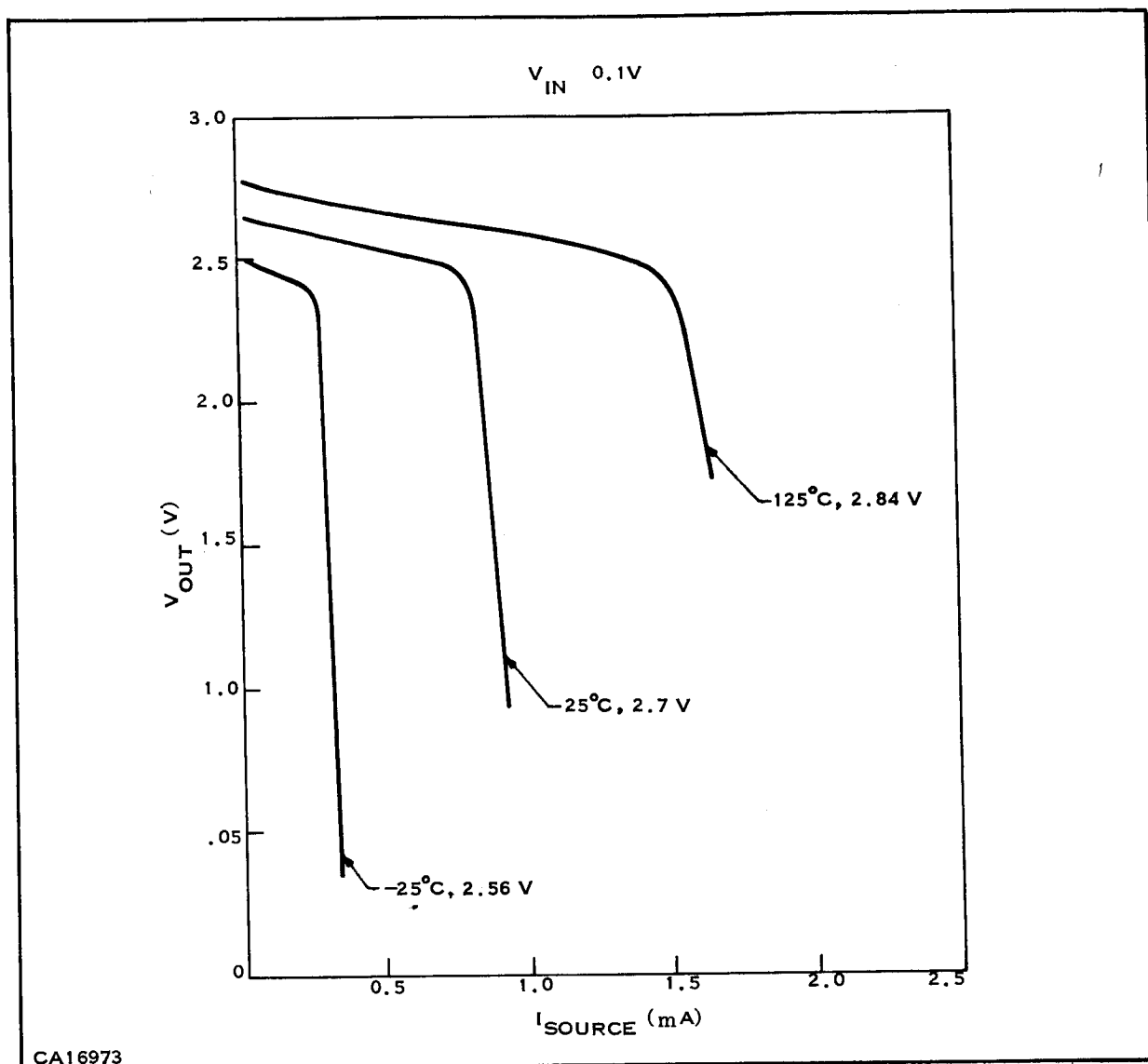
Figure 59. V_{OUT} versus I_{SOURCE} (MS-71)

gain of the gating transistor Q3. This current is not detrimental to circuit operation but it is a significant portion of the "0" standby power. From Figures 68 and 69, it is seen that this current is greater than 10% of the specified 300 μW.

3. Flip-Flop Characterization—Schedule A Process

A series of 12 tests were used to characterize the Flip-Flop circuit. In all tests except the last two, the Flip-Flop was operated as a counter. In the counter configuration, the J and K inputs as well as the dc Set and Reset inputs were returned to V_{CC}, the worst-case power consideration.

The method of specifying transient performance of the Flip-Flop will be to quote the delay, rise and fall times.
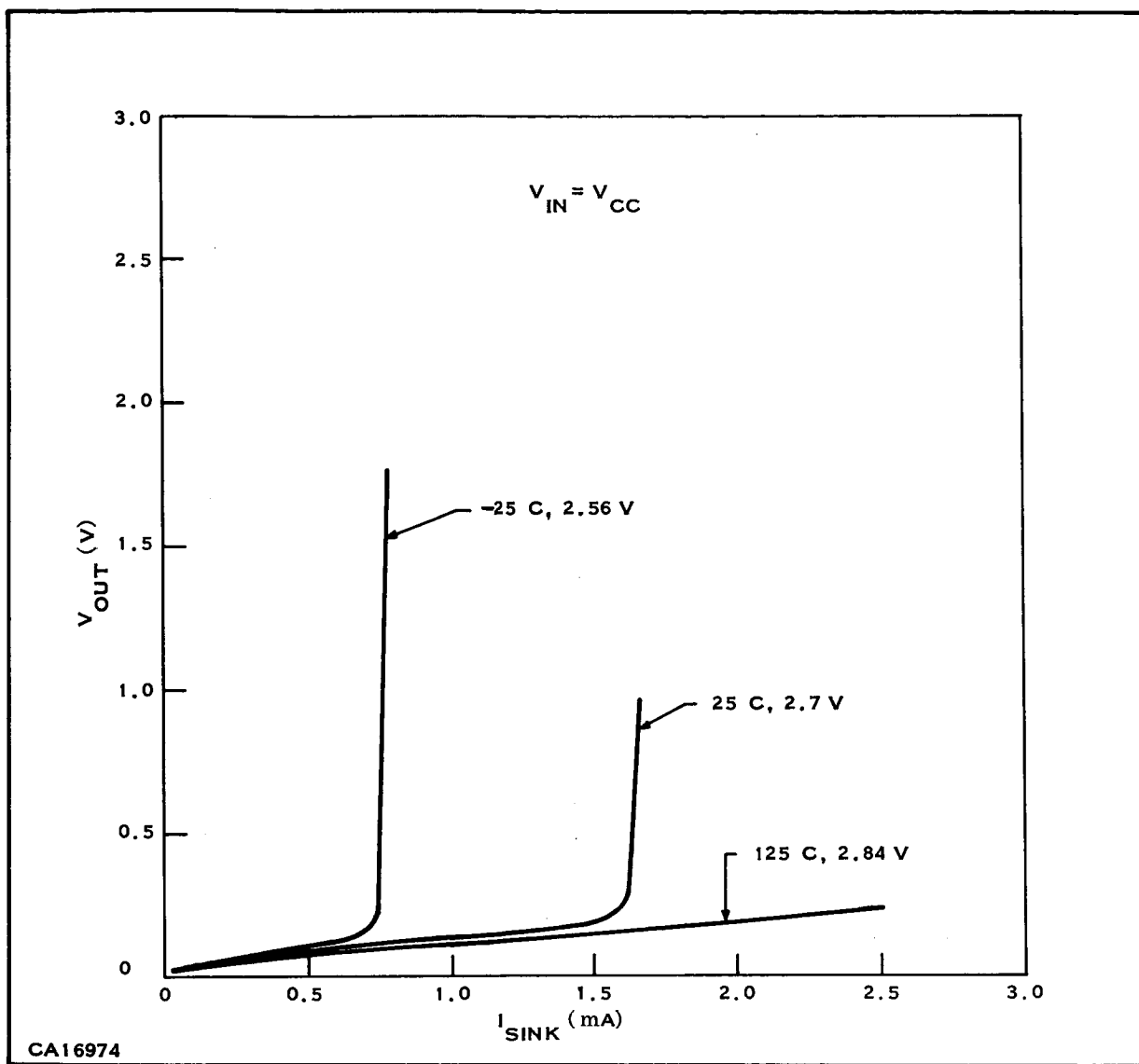
Figure 60. V_{OUT} versus I_{SINK} (MS-4)

The propagation delay time (t_p) is defined as the average of the delays for both the leading and trailing edges of the output waveform. This Flip-Flop changes states on the negative going portion of the clock; therefore, the delay times will be referenced from the trailing edges of the input voltage pulse. Using the waveforms of Figure 70, the following definitions apply: The delay time t_{pd0} is the time difference between that time when the input pulse reaches 50 percent down from its initial value (trailing edge) and the time when the output has fallen to its 50 percent point. Similarly, the delay time, t_{pd1}, is the time between the 50 percent points as the output goes high. The propagation delay is defined as the average of the two delays, i.e.,

$$t_p = \frac{t_{pd0} + t_{pd1}}{2}$$

The rise and fall times are defined in the same manner as in paragraph IIF2.
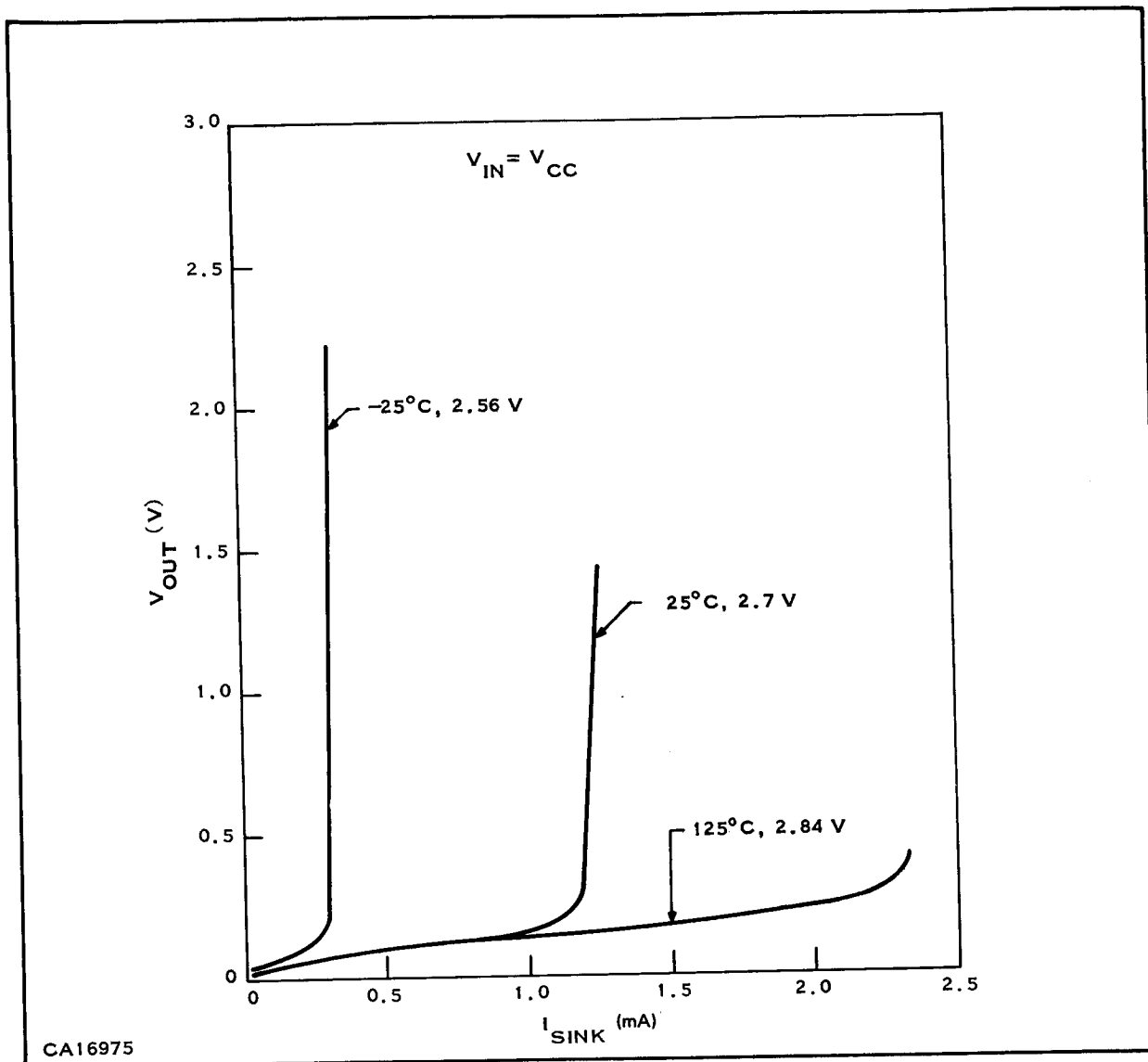
Figure 61. V_{OUT} versus I_{SINK} (MS-71)

The data for two circuits will be present. The first Flip-Flop (MF-92) was fabricated in lot MF-AJ. The second Flip-Flop (MF-156) was fabricated in lot MF-AP. Both circuits are typical of the Flip-Flops fabricated on this contract. Titles of figures showing Flip-Flop performance are listed here for convenient reference and followed by comments on the performance.

Figure 71—Standby Power versus V_{CC} (MF-92)
Figure 72—Standby Power versus V_{CC} (MF-156)
Figure 73—Frequency versus Power (MF-92)
Figure 74—Frequency versus Power (MF-156)
Figure 75—Power versus Temperature (MF-92)
Figure 76—Power versus Temperature (MF-156)
Figure 77—Switching Waveform, t_{pd0} (MF-92)

Figure 62. V_{IN} versus I_{IN} (MS-4)

NO LOAD

125°C, 2.84 V

25°C, 2.7 V

−25°C, 2.56 V

V_{IN} (V)

I_{IN} (μA)

CA16977

Figure 63. V_{IN} versus I_{IN} (MS-71)

Figure 90–DC Set and Reset (MF-92)
Figure 91–DC Set and Reset (MF-156)

The tests were conducted using the Flip-Flop as a counter. The clock input was driven by the same drive gate used in the NAND gate test. The counter will give worst-case power conditions.

A few comments will again be made on the data presented. The standby power plots of Figures 71 and 72 show that the circuits are within the 300 μW specification. Maximum frequency for Flip-Flop operation is reduced from that of the NAND gate circuits to obtain the 300-μW specification. The Flip-Flop can be thought of as consisting of two ON inverters and one ON AND section in either state. To remain under 300 μW, the power of the AND section was reduced, thus reducing the upper operating frequency. Figures 73 and 74 show that the 2 MHz F_{max} specification
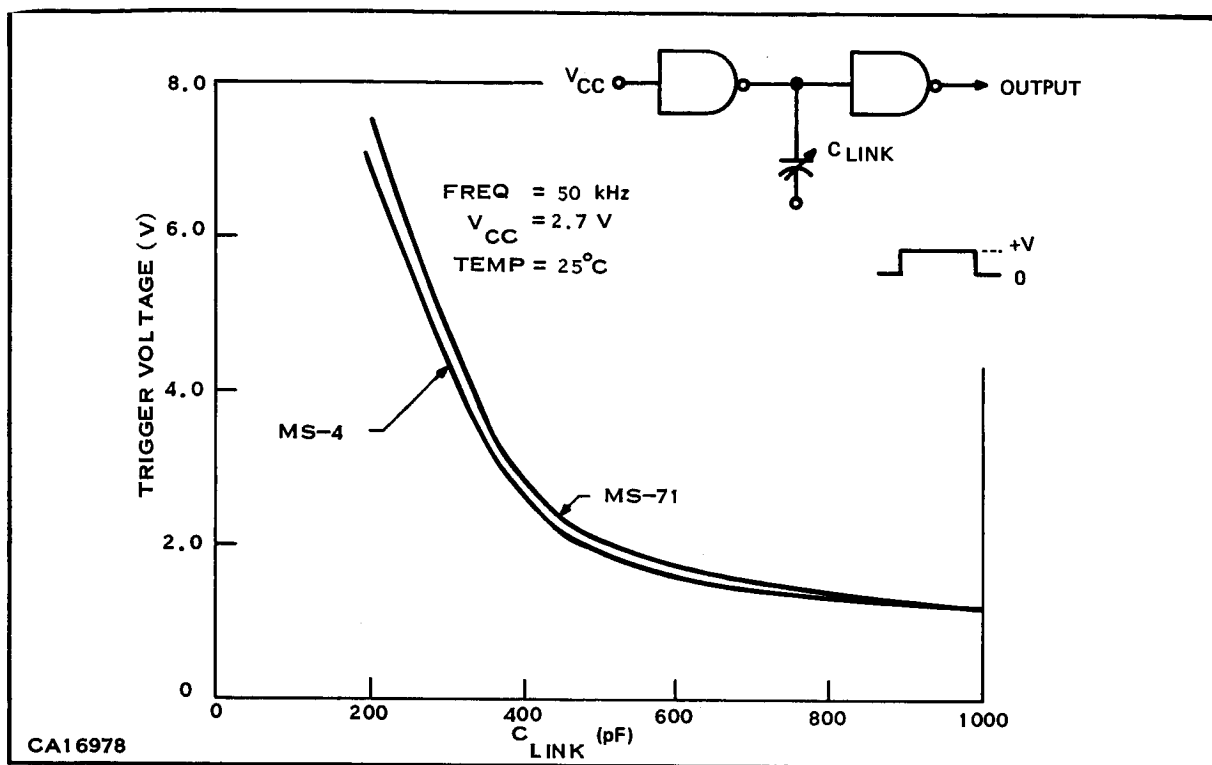
Figure 64. AC Noise (MS-4, MS-71)

was not met, but 1 MHz was realized under all conditions. This again shows a 100% increase over the circuits fabricated during contract NAS1-4350.

The switching waveforms of Figures 77 through 80 completely describe the circuit transient response. Conditions shown are for NO LOAD, 5 Flip-Flops and 5 NAND gates. All V_{CC} voltages are 2.7 V. Both delay times are approximately equal. Notice that the propagation delay varies little with increased power (Figure 81).

The maximum operating frequency (F_{max}) plot of Figure 82 was obtained by varying V_{CC} from 2.0 to 6.0 V. The power is the power at F_{max}. The effect of load capacitance is shown in Figure 83.

Output characteristics (V_{OUT} versus I_{SOURCE} and I_{SINK}) are shown in Figures 84 through 87. Notice that the PNP transistor of MF-92 (see Figure 84) has a somewhat lower h_{FE} than does the same transistor of unit MF-156 (see Figure 85). The 500 μA was achieved under all conditions. Again the output impedance was the R_{sat} of the transistors until the devices were pulled out of saturation.

Trigger sensitivity for the Flip-Flops is shown in Figures 88 and 89. They are plotted over a wide range of trigger fall times.
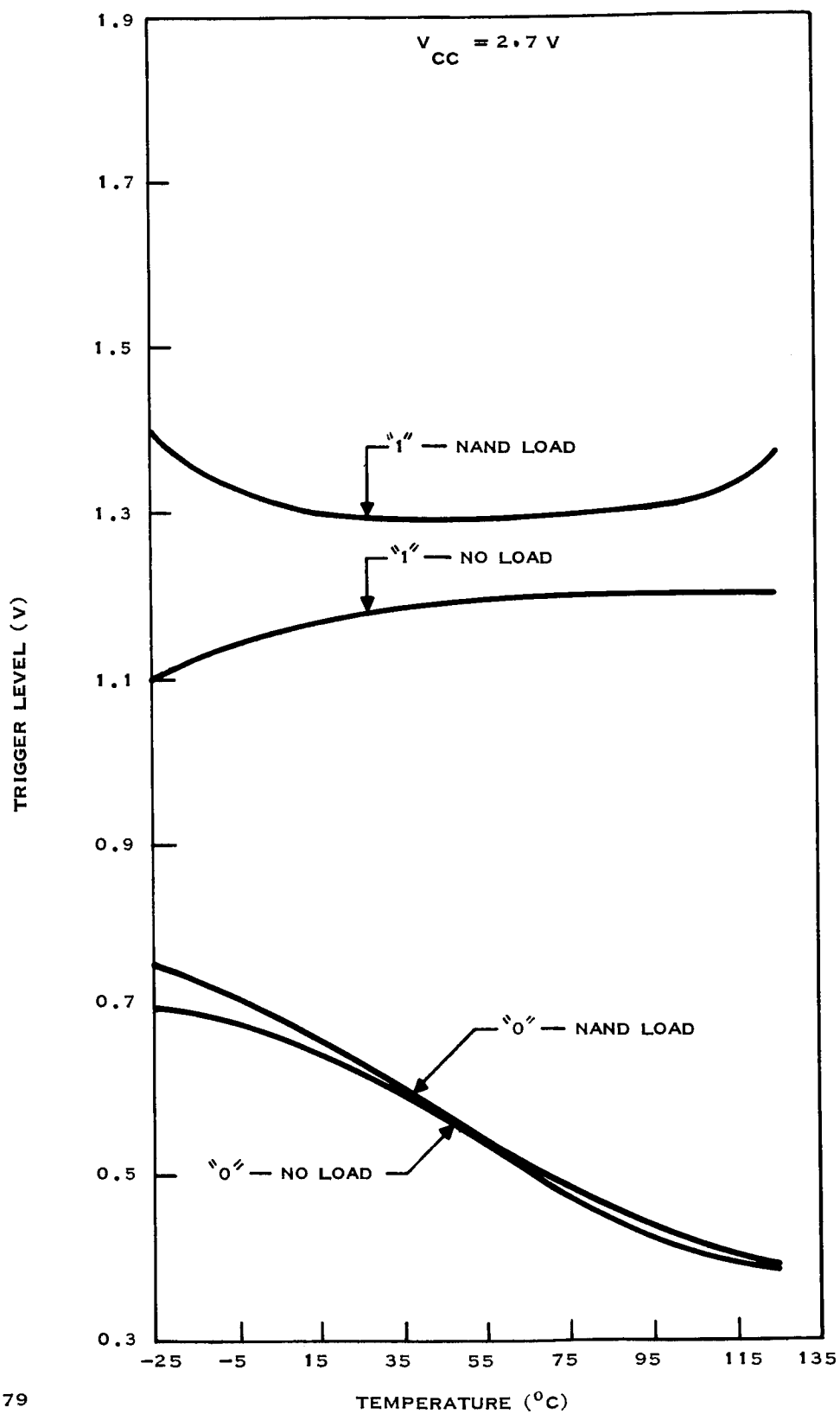
Figure 65. Trigger Level versus Temperature (MS-4)
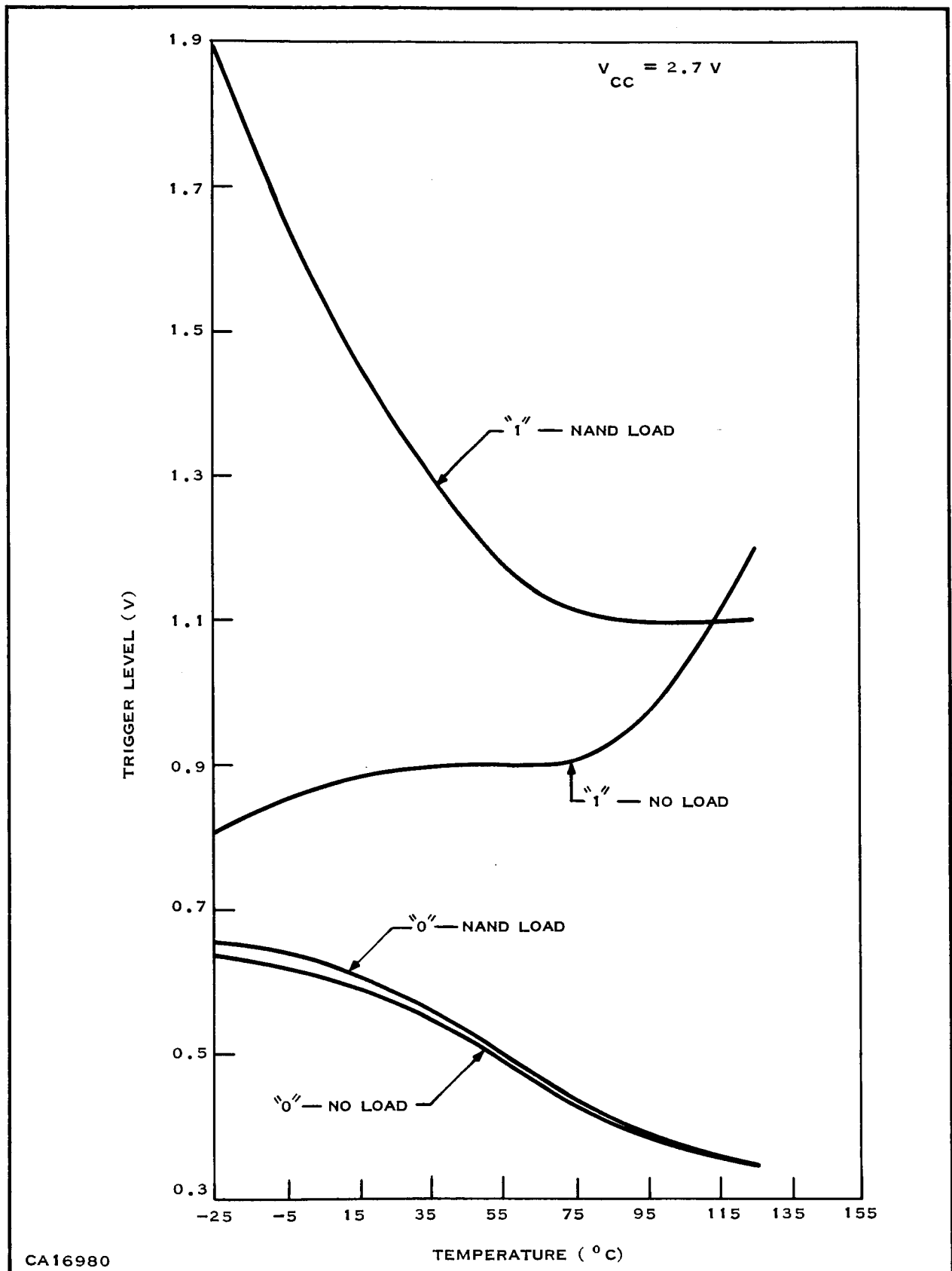
Figure 66.   Trigger Level versus Temperature (MS-71)
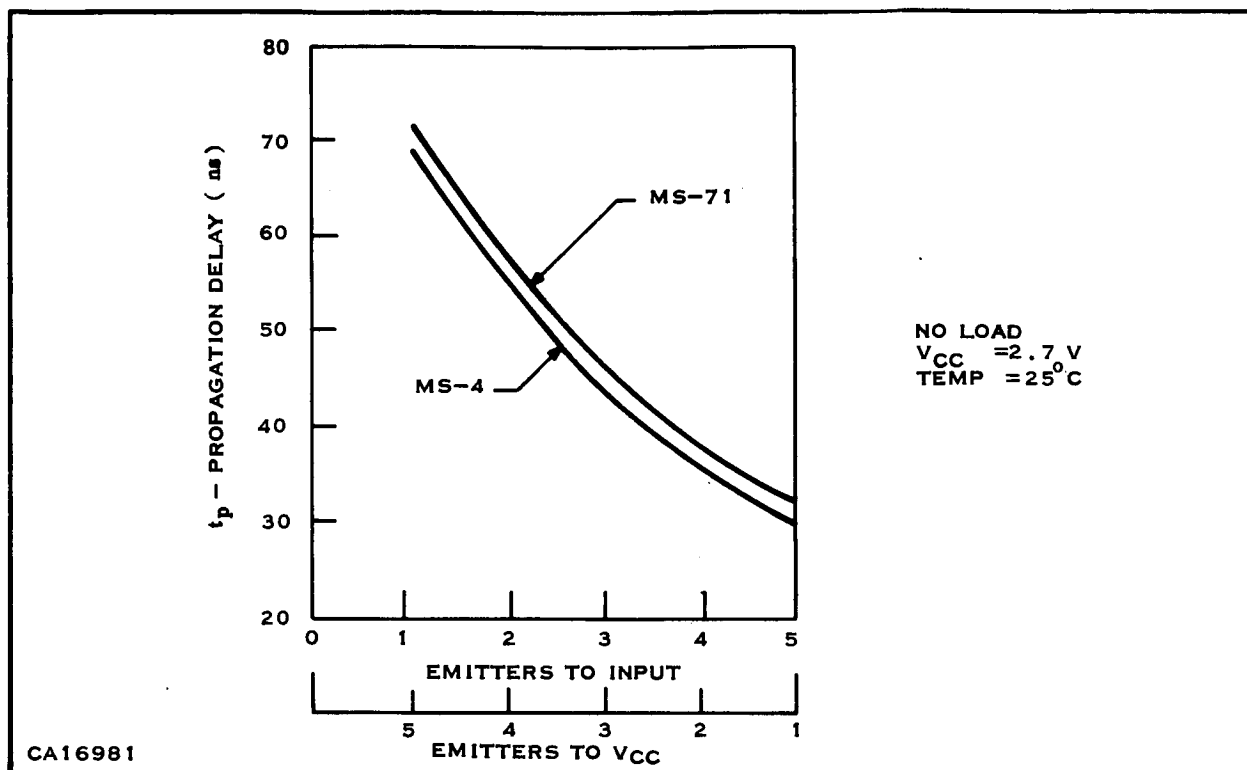
Figure 67.   Propagation Delay versus Emitters to V_{CC} (MS-4, MS-71)

Figures 90 and 91 are the resulting waveforms of an input at the dc Set and Reset terminals. The delay times will be defined in a manner similar as to when the input is at the clock (see Figure 70). The delay times are tabulated for the conditions listed in Table I.

The J-K input characteristics were determined by using the following test sequence:

1)   50 kHz on clock input.

2)   Set K to V_{CC}, J to ground.

3)   Set K to ground, J remains at ground—Q should be at a "0".

4)   Hold K to ground, increase voltage to J and observe voltage at which Q goes to a "1". This will be called the J level.

5)   Increase voltage at J until it reaches V_{CC}.

6)   Increase voltage at K until circuit acts as a counter. This will be called the K level.

The results of these tests, along with the conditions are listed in Table II.

4.   Schedule B Process Circuits

As pointed out earlier in this section, circuits would be fabricated using both Schedule A and Schedule B processes. The major effort was directed toward Schedule A, but a few circuits using

Table I. DC Set and Reset Switching Times

Device No.	Temperature (°C)	t_{pd1} (ns)	t_{pd0} (ns)	V_{CC} (V)
92	−25	80	133	2.7
92	25	65	117	2.7
92	125	63	120	2.7
156	−25	57	123	2.7
156	25	52	117	2.7
156	125	55	125	2.7

Table II. J-K Input Characteristics

Device No.	Temperature (°C)	V_{CC} (V)	J level (V)	K level (V)
92	−25	2.56	0.75	0.85
92	25	2.7	0.6	0.7
92	125	2.84	0.35	0.45
156	−25	2.56	0.8	0.9
156	25	2.7	0.65	0.7
156	125	2.84	0.4	0.4
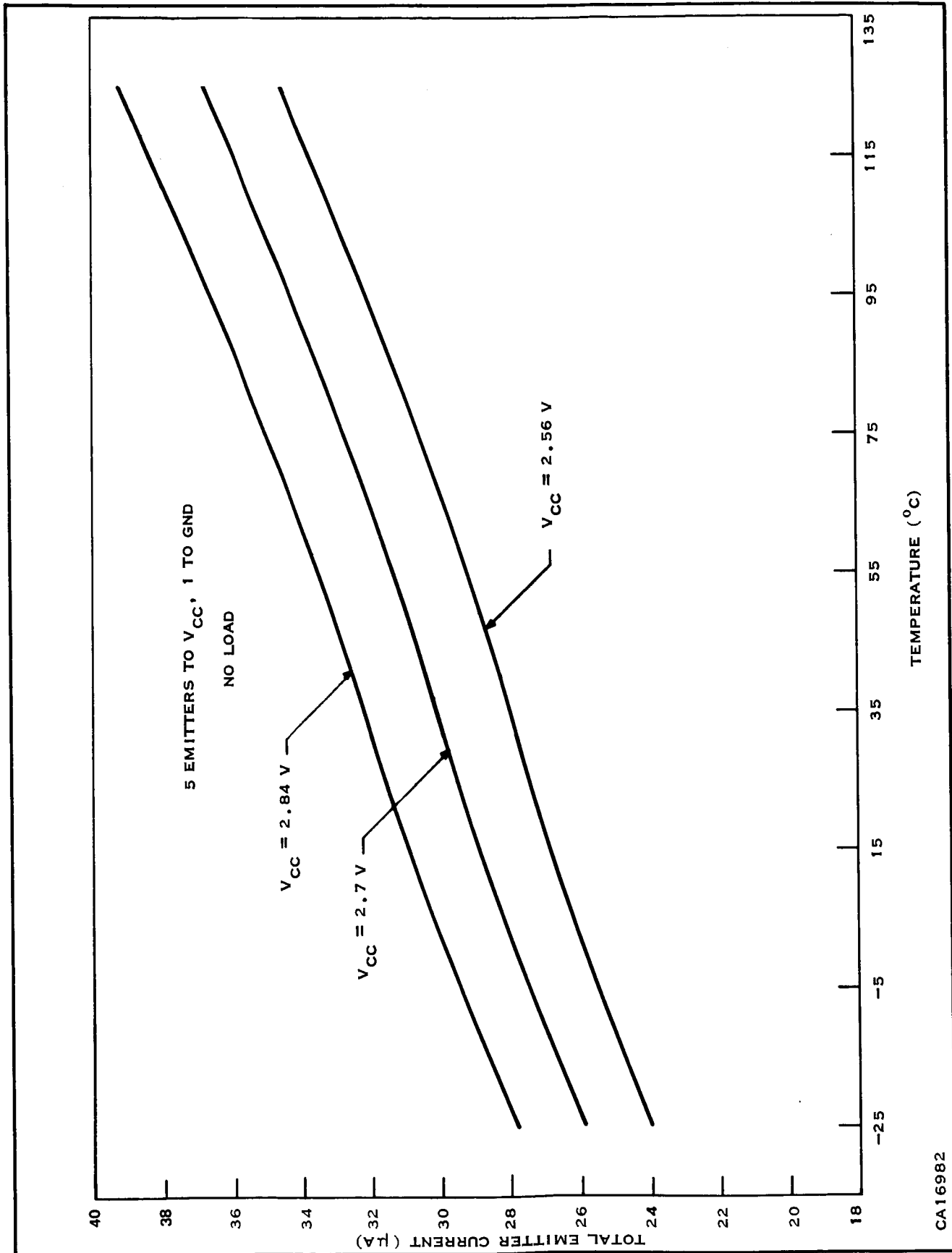
Figure 68.   Current Due to Emitters at V_{CC} (MS-4)

Figure 69. Current Due to Emitters at V_{CC} (MS-71)

CA16983
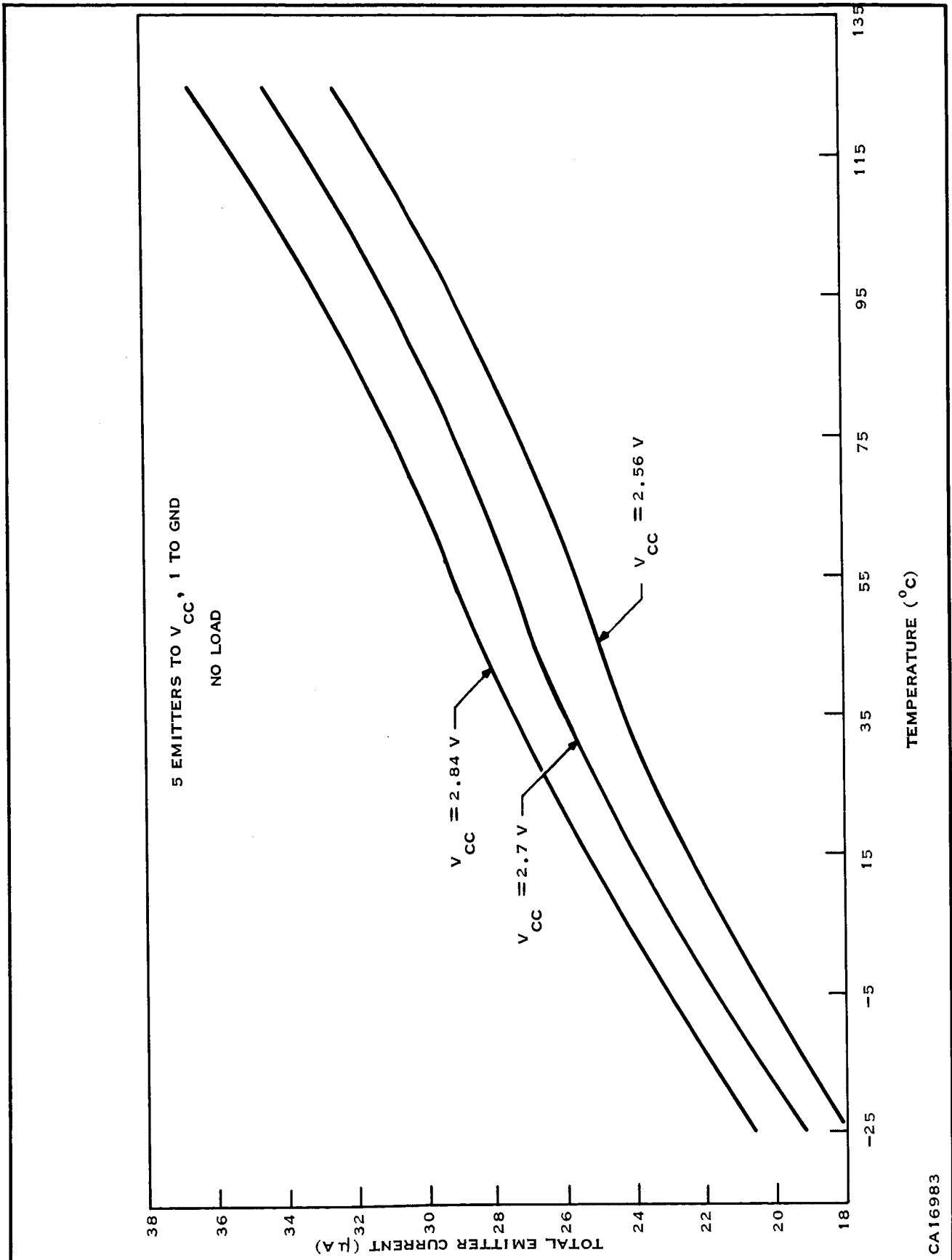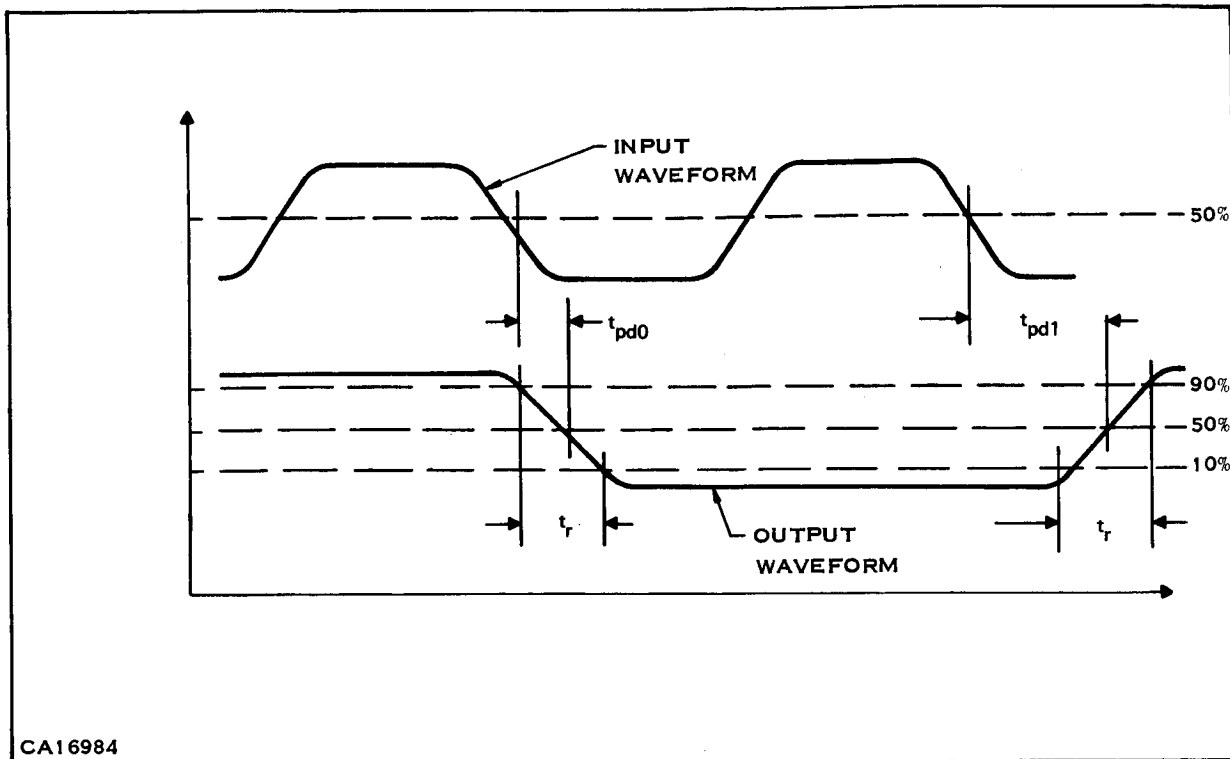
Figure 70.   Definition of Switching Times (Flip-Flop)

Schedule B were made. No mask changes were required; only a materials schedule manipulation was needed. A limited amount of circuit data was taken for Schedule B since the only change was in the PNP devices. The purpose of Schedule B was not to increase circuit performance, but to obtain a more consistent PNP device. Figures 92 and 93 are frequency-versus-power plots along with "0" and "1" standby power for the NAND gates and Flip-Flops respectively. This data was taken at NO LOAD, V_{CC} = 2.7 V and 25°C temperature. The switching waveforms for the same condition are shown in Figures 94 and 95. Very little difference in overall characteristics was noticed between the two schedules. Little difference was expected. The objective was to simplify the fabrication process.
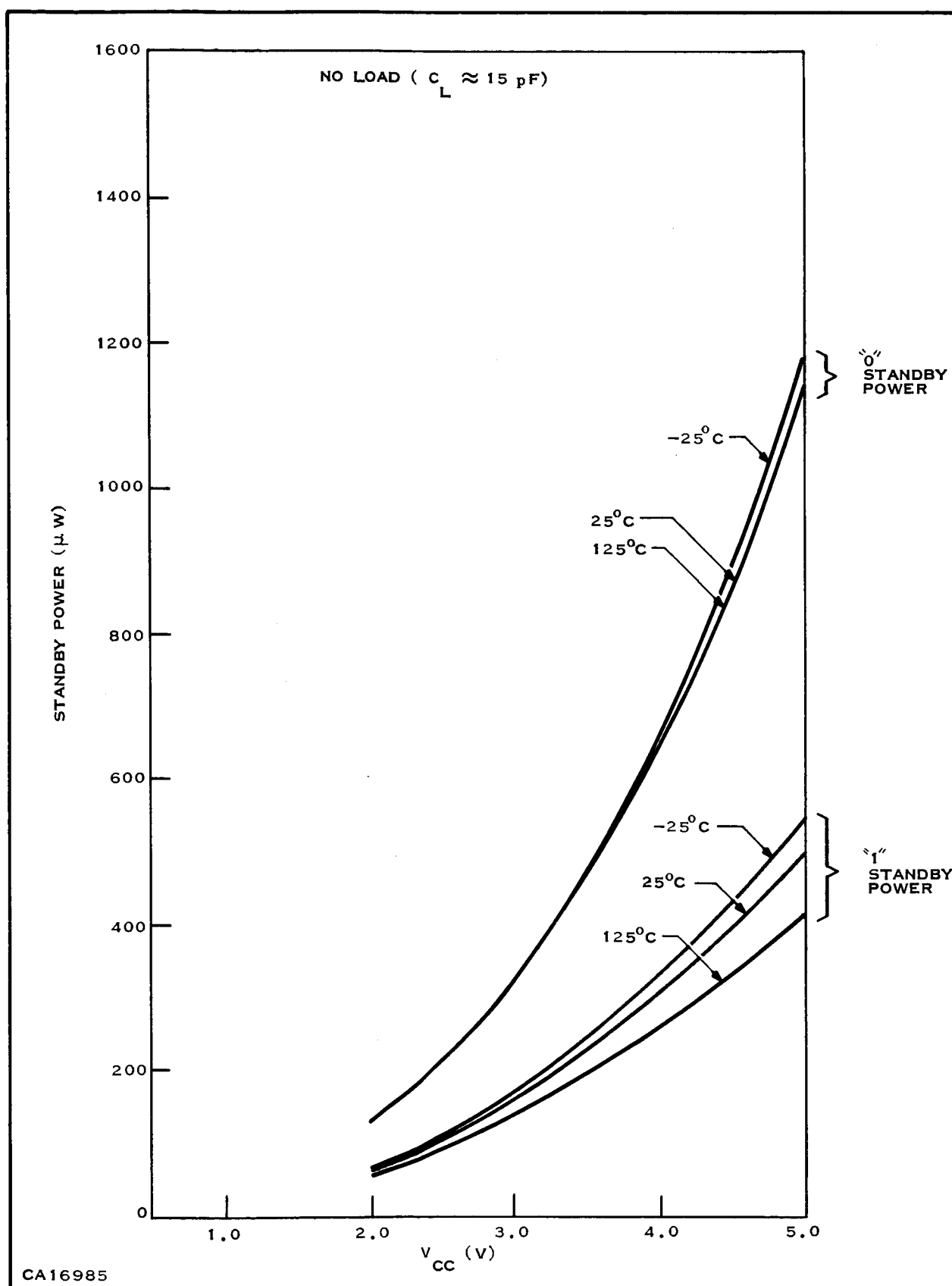
Figure 71.   Standby Power versus V_{CC} (MF-92)
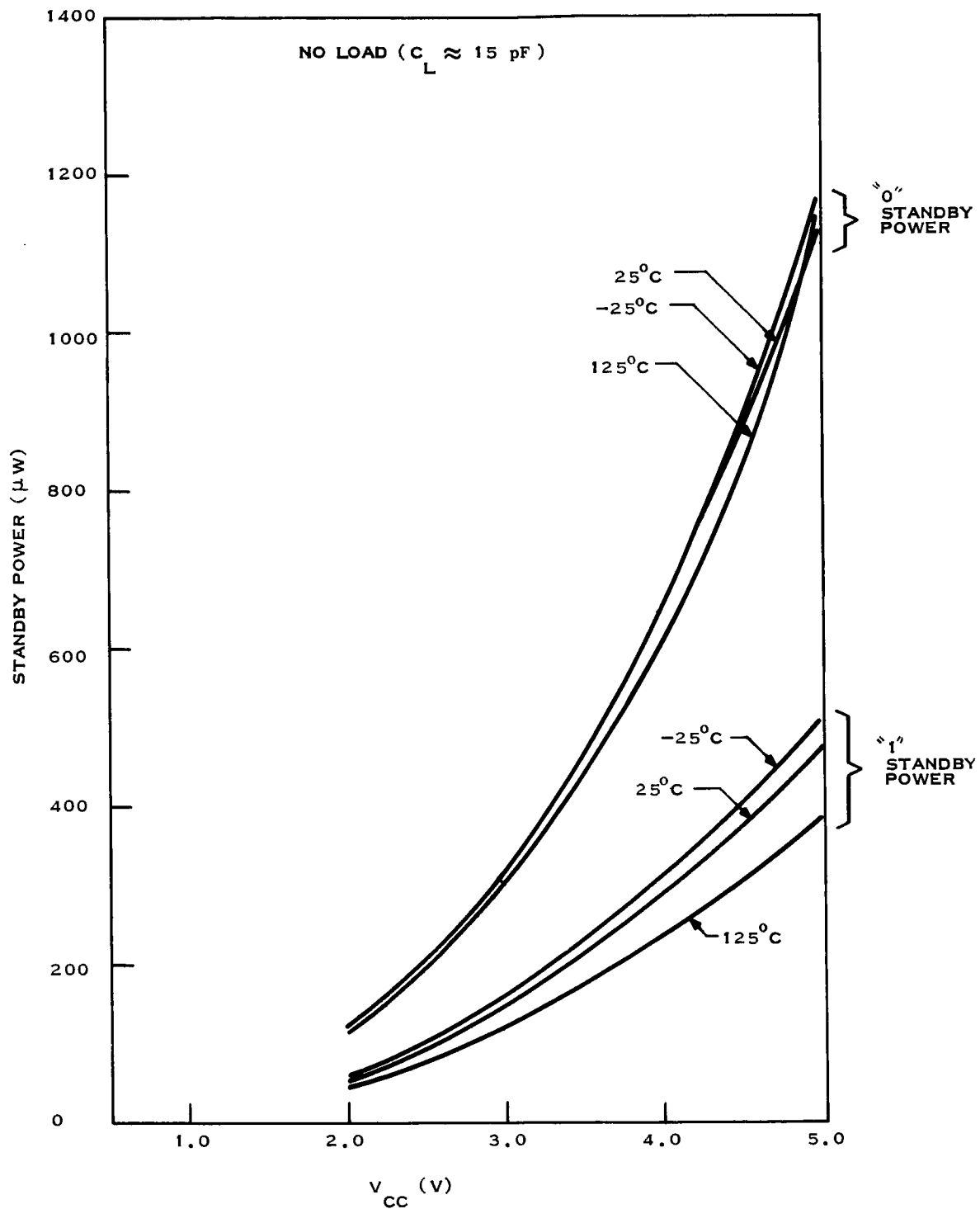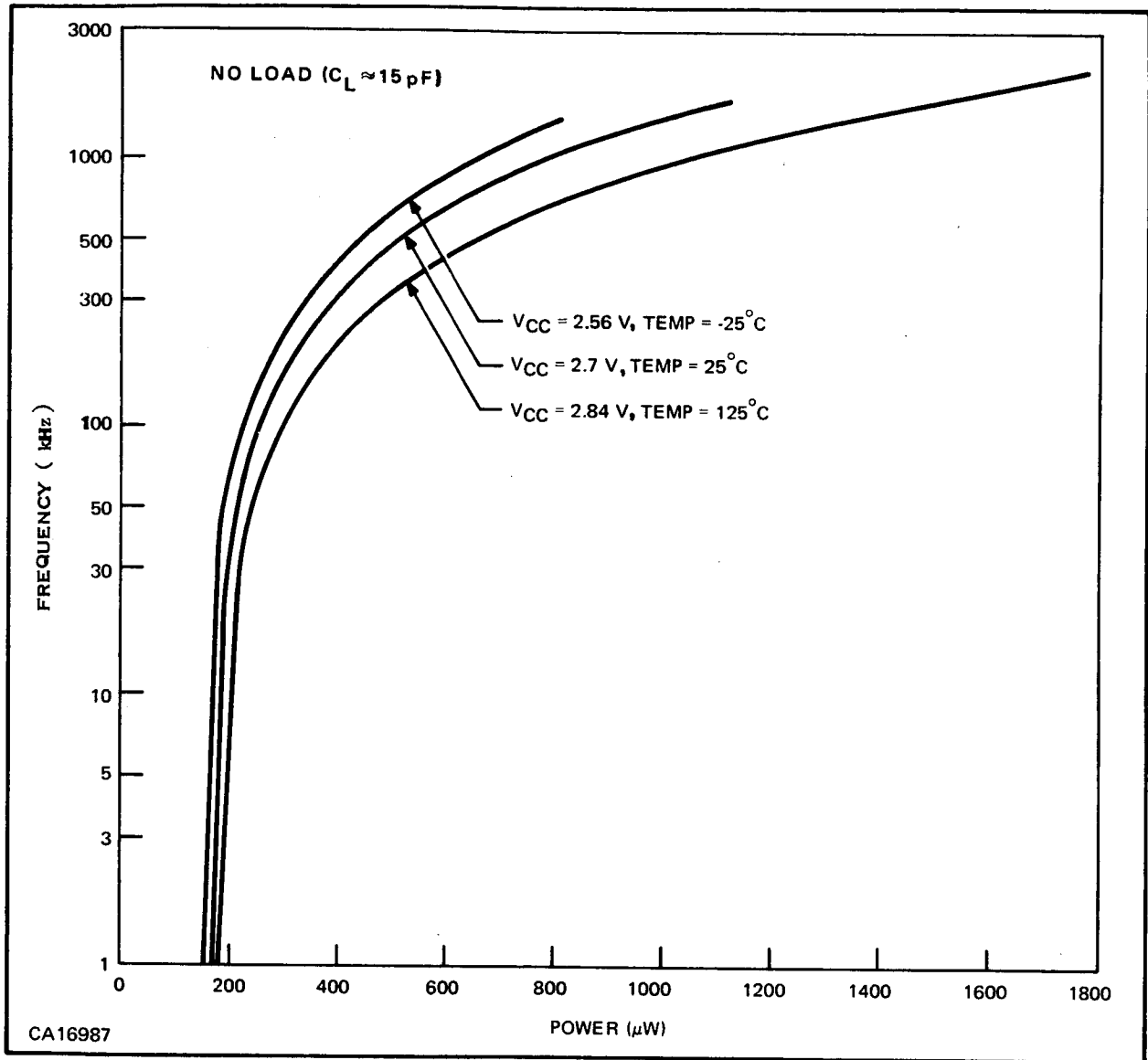
Figure 72. Standby Power versus V_{CC} (MF-156)

Figure 73. Frequency versus Power (MF-92)

Figure 74.   Frequency versus Power (MF-156)

Figure 75. Power versus Temperature (MF-92)

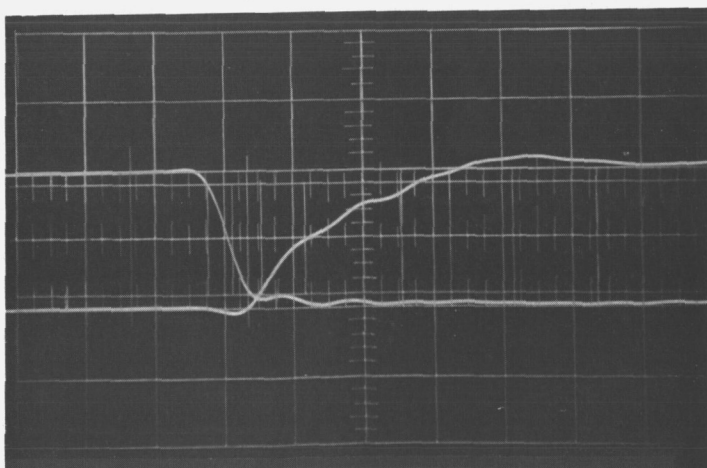Figure 76. Power versus Temperature (MF-156)

CA16990
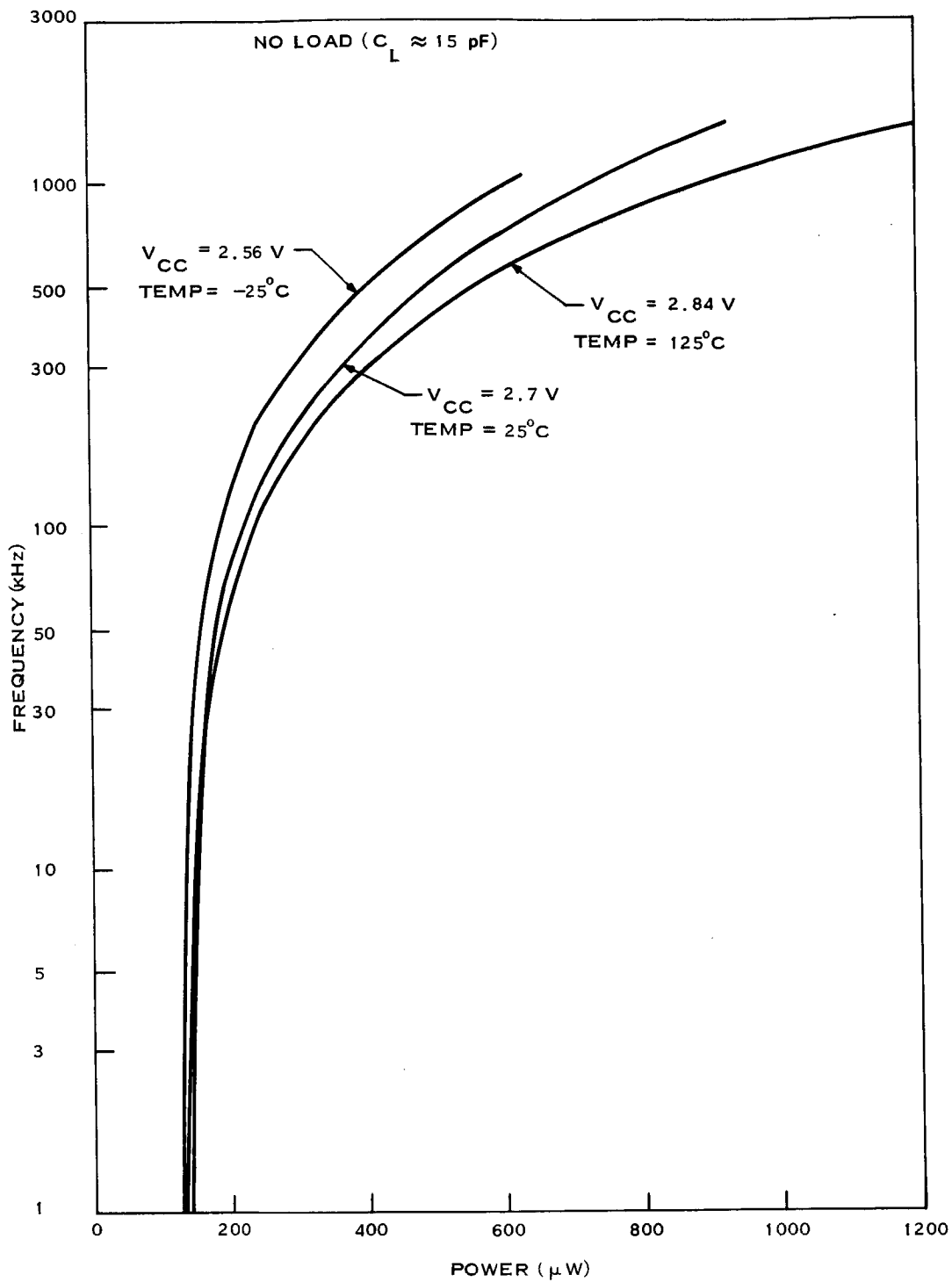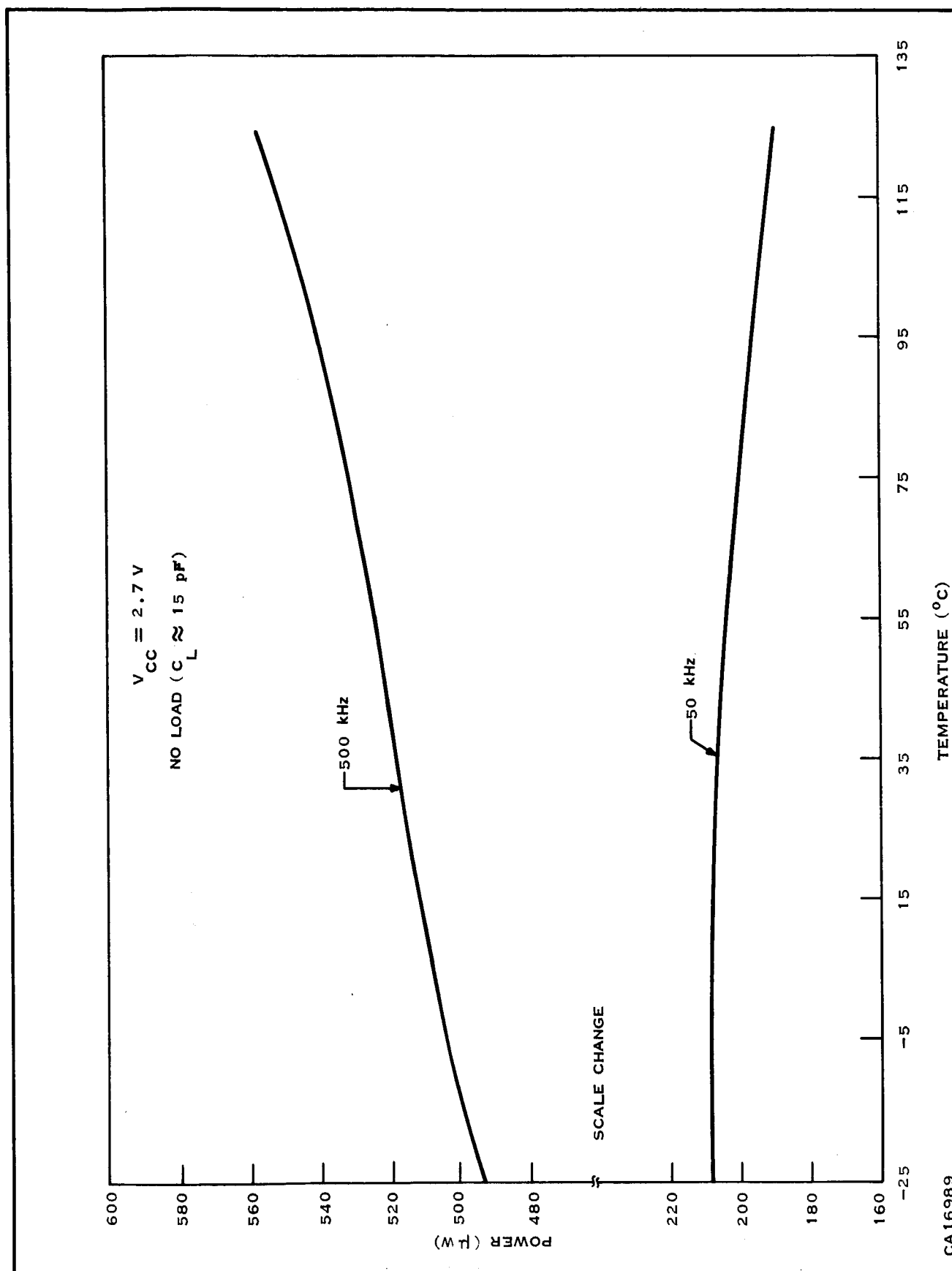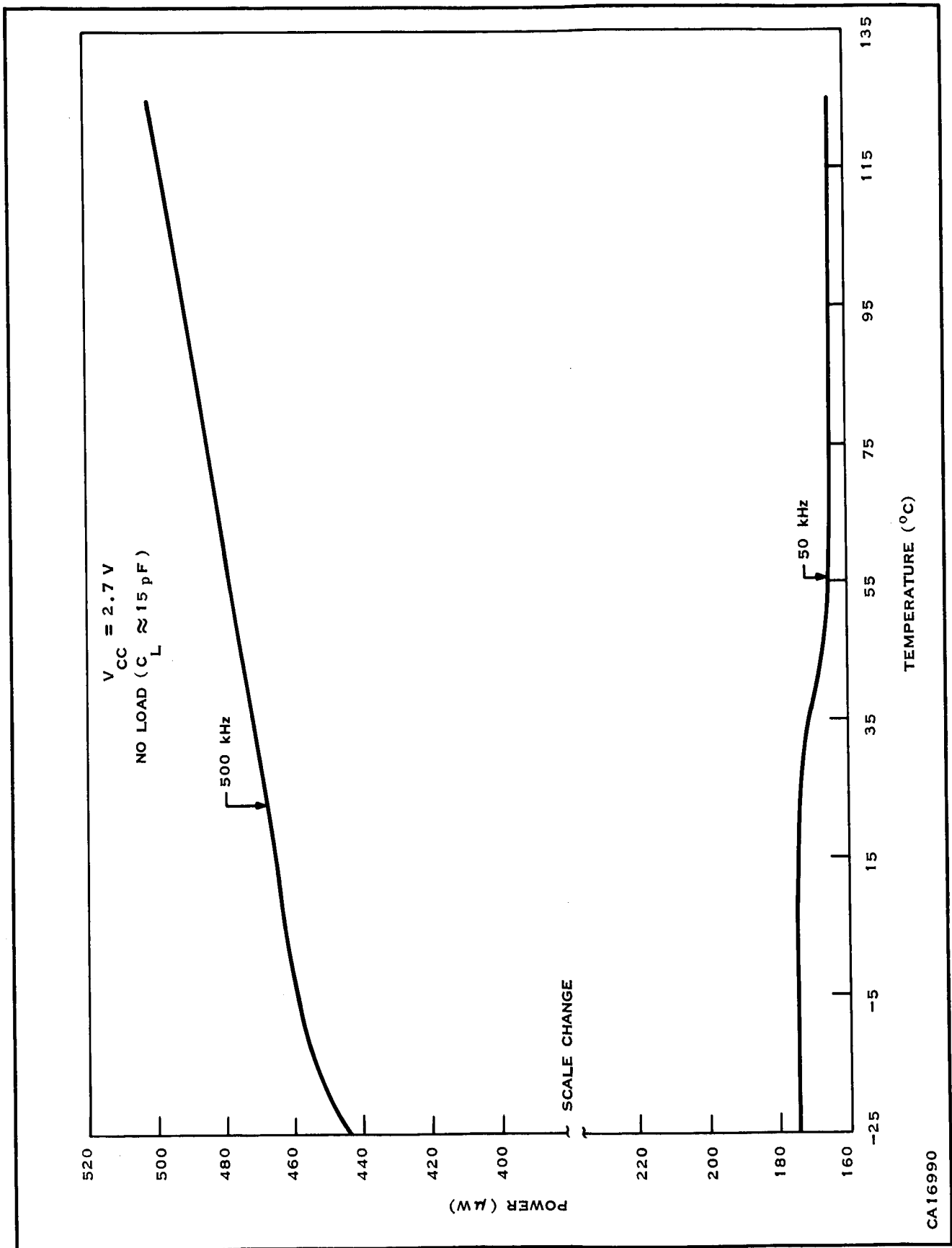
(a.) NO LOAD
20 ns /DIV
-25°C
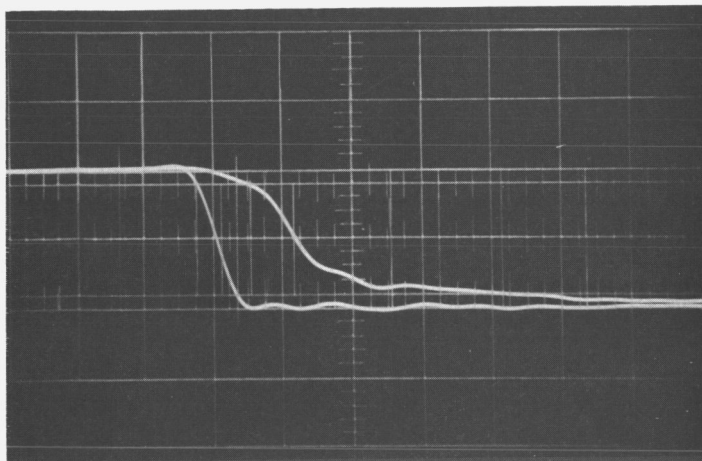
(b.) FLIP-FLOP LOAD
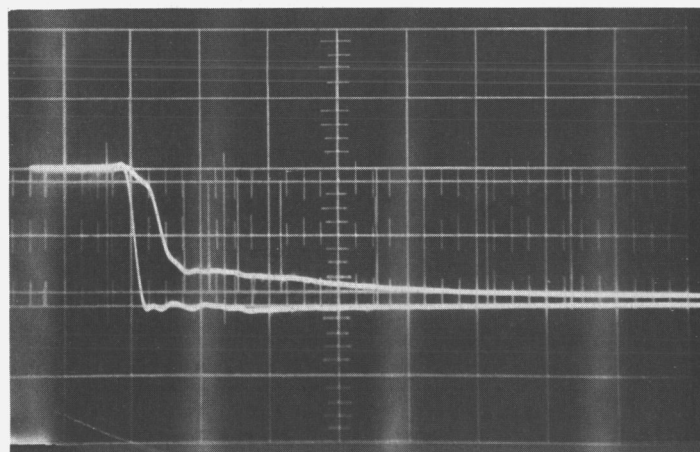50 ns /DIV
-25°C
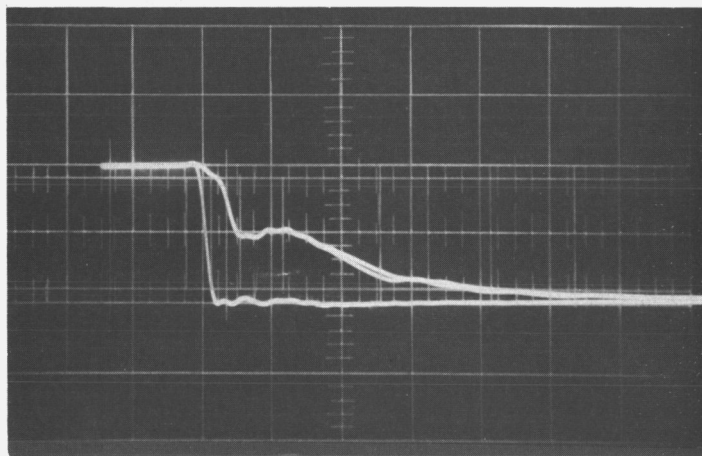
(c.) NAND LOAD
50 ns /DIV
-25°C
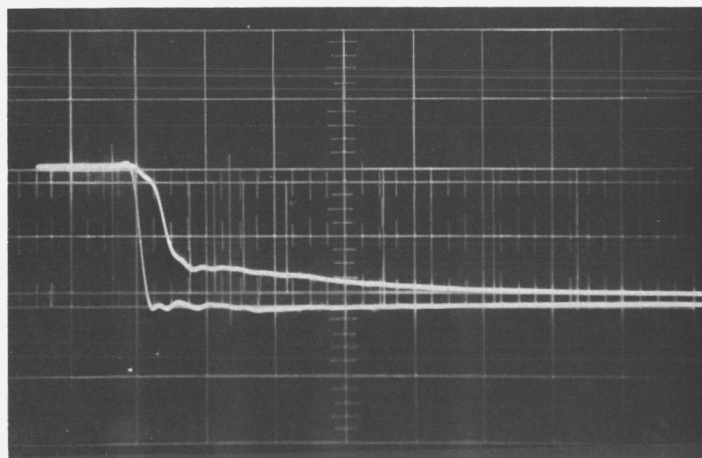
CA16903(1-3)

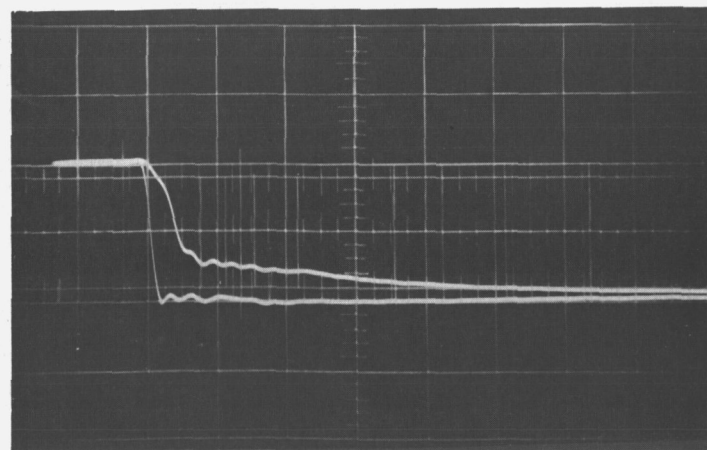**Figure 77.** Switching Waveform — t_{pd0} (MF-92)
(Sheet 1 of 3)

(d.) NO LOAD
20 ns/DIV
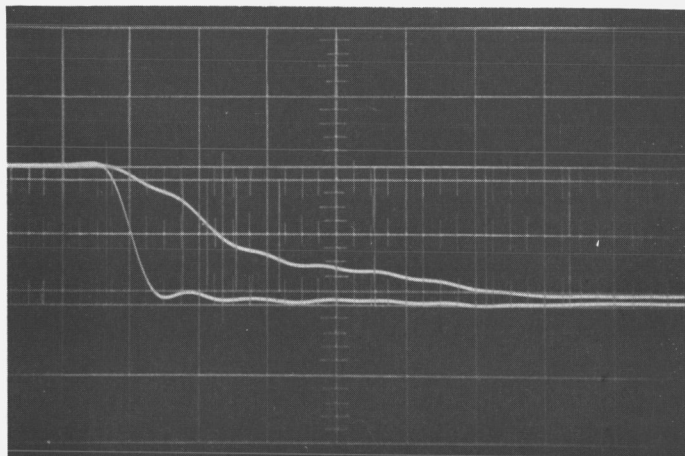25°C
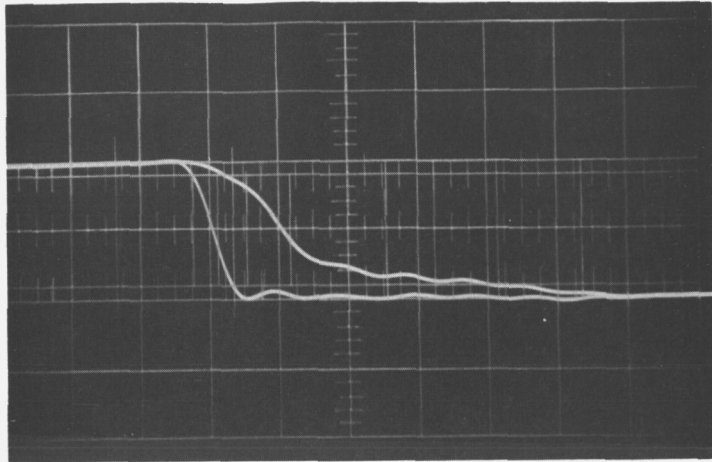
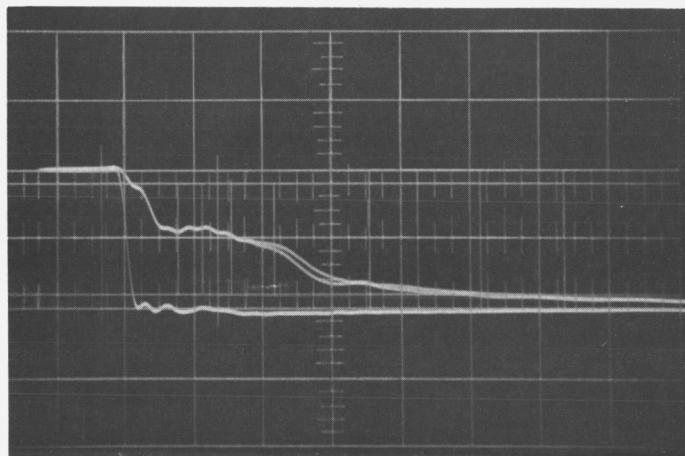(e.) FLIP-FLOP LOAD
50 ns/DIV
25°C
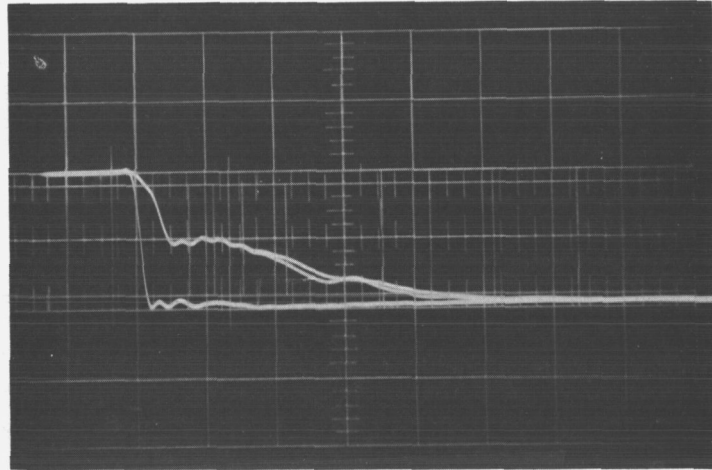
(f.) NAND LOAD
50 ns/DIV
25°C
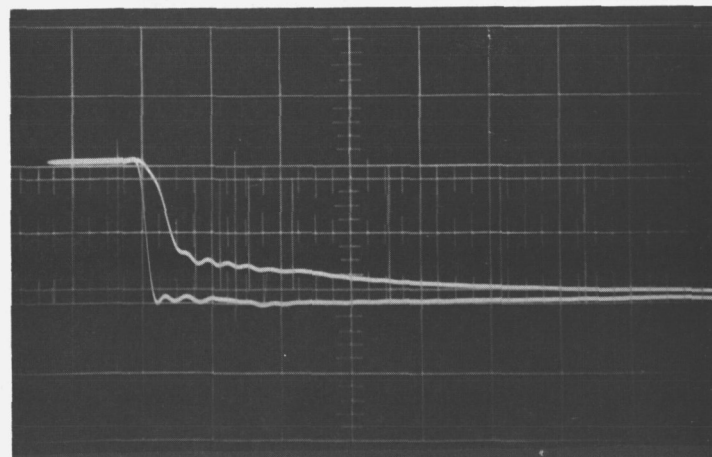
CA16903(2-3)

Figure 77. Switching Waveform — t_{pd0} (MF-92)
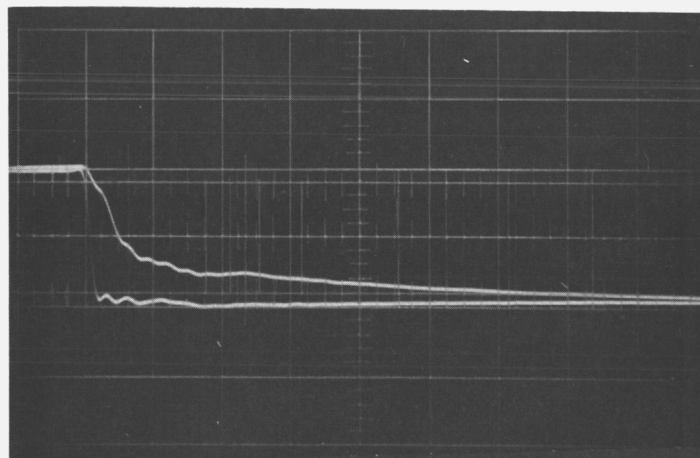(Sheet 2 of 3)

(g.) NO LOAD
20 ns/DIV
125°C
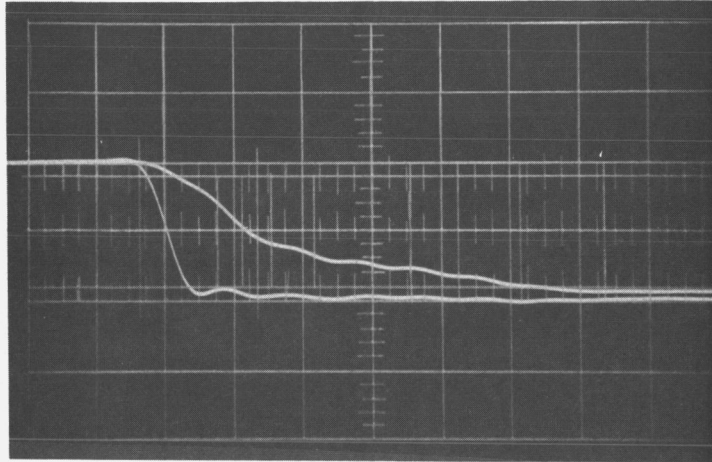
(h.) FLIP-FLOP LOAD
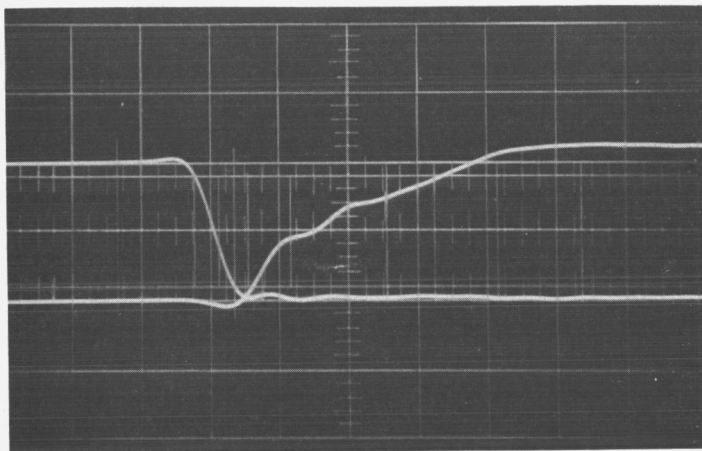50 ns/DIV
125°C
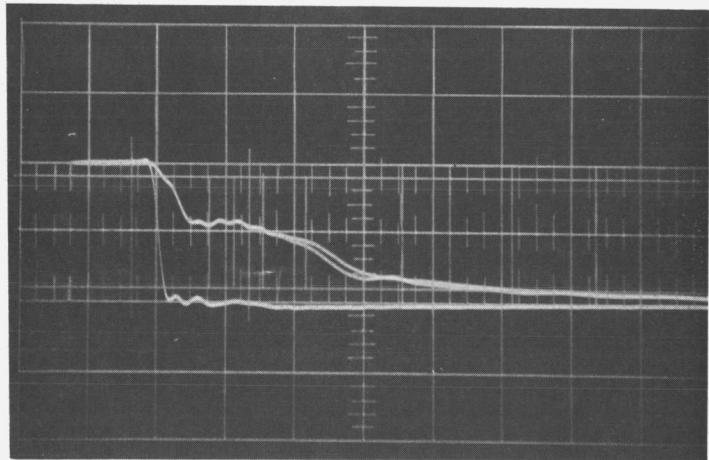
(i.) NAND LOAD
50 ns/DIV
125°C
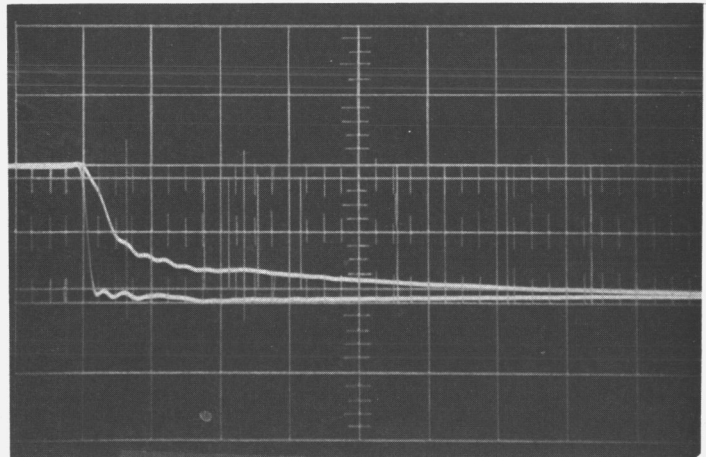
CA16903(3-3)

Figure 77.   Switching Waveform − t_{pd0} (MF-92)
(Sheet 3 of 3)

(a.) NO LOAD
20 ns /DIV
-25°C
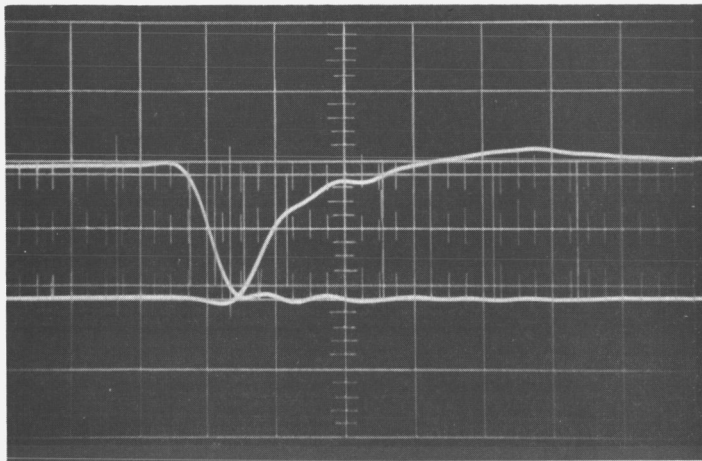
(b.) FLIP-FLOP LOAD
20 ns /DIV
-25°C
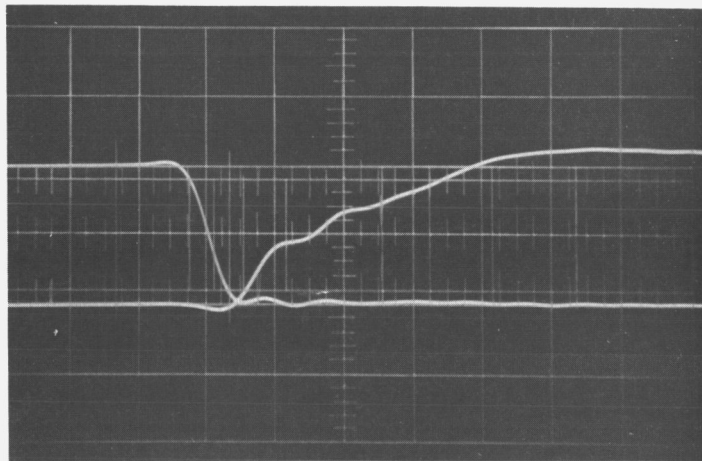
(c.) NAND LOAD
20 ns /DIV
-25°C
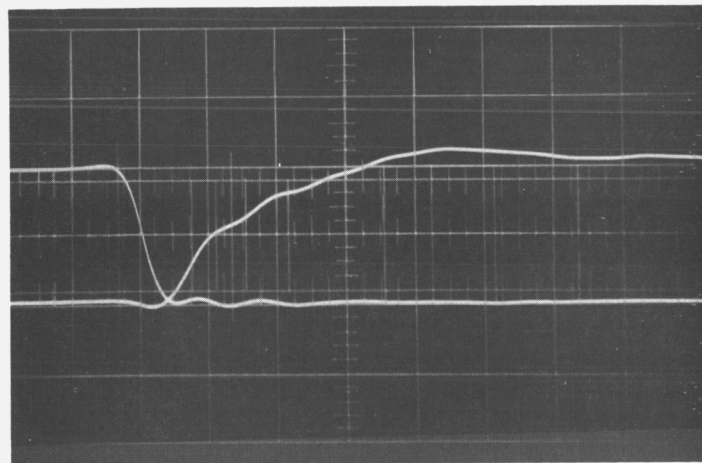
CA16904)1-3)

Figure 78. Switching Waveform − t_{pd1} (MF-92)
(Sheet 1 of 3)

(d.) NO LOAD
20 ns/DIV
25°C
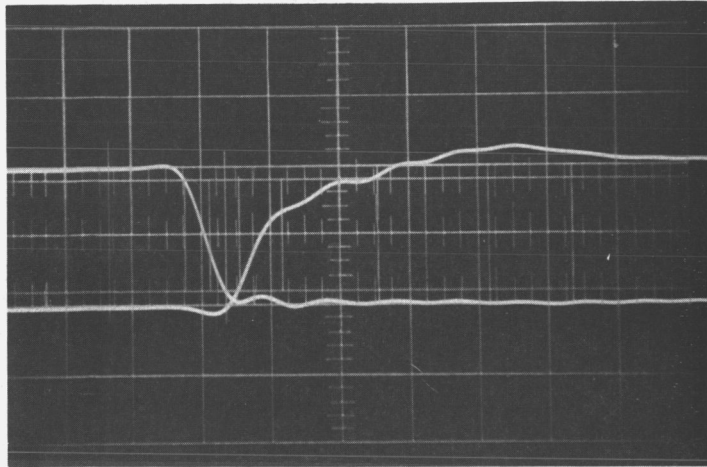
(e.) FLIP-FLOP LOAD
20 ns/DIV
25°C
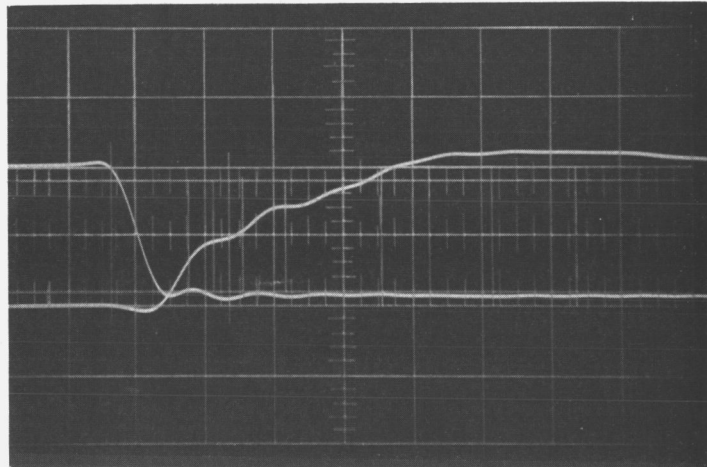
(f.) NAND LOAD
20 ns/DIV
25°C
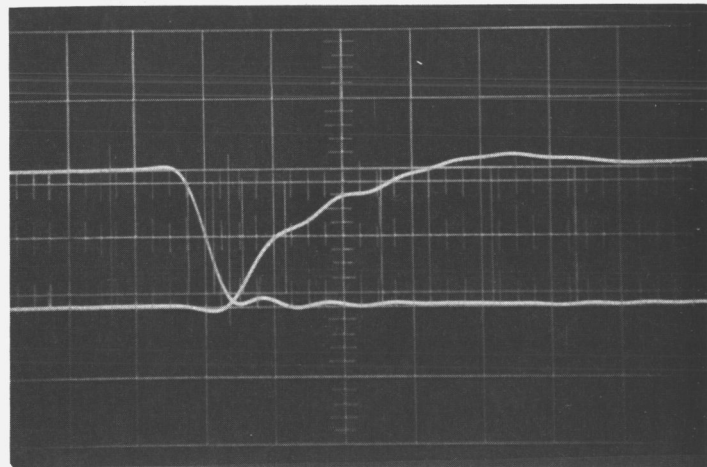
CA16904(2-3)

Figure 78.   Switching Waveform — t_{pd1} (MF-92)
(Sheet 2 of 3)

(g.) NO LOAD
20 ns/DIV
125°C
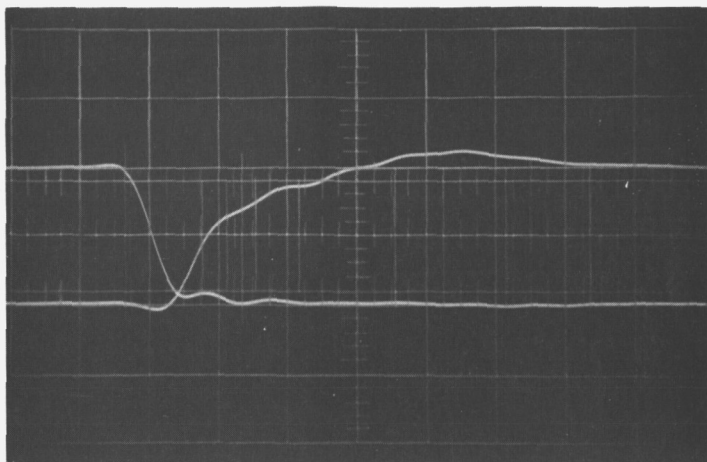
(h.) FLIP-FLOP LOAD
20 ns/DIV
125°C
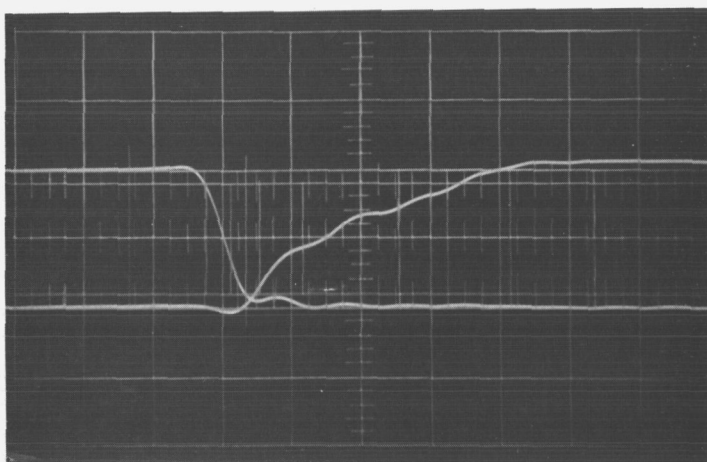
(i.) NAND LOAD
20 ns/DIV
125°C

CA16904(3-3)

Figure 78.   Switching Waveform − t$_{pd1}$ (MF-92)
(Sheet 3 of 3)

(a.) NO LOAD
20 ns /DIV
-25°C
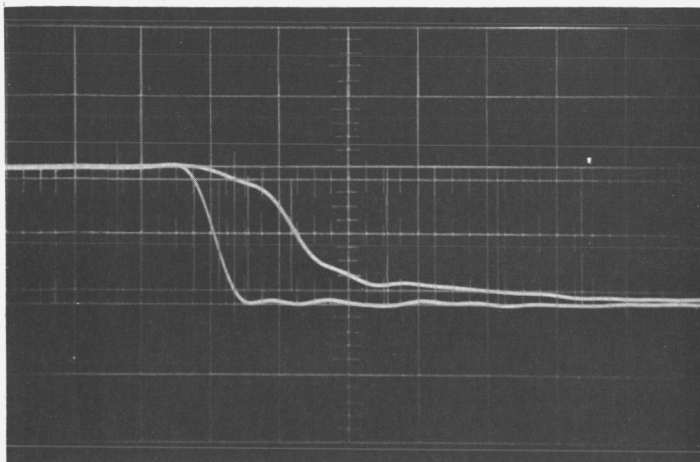
(b.) FLIP-FLOP LOAD
50 ns /DIV
-25°C
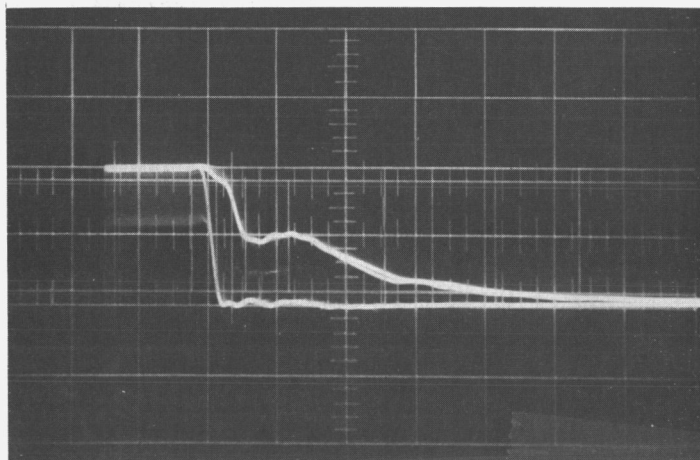
(c.) NAND LOAD
50 ns /DIV
-25°C

CA16905(1-3)

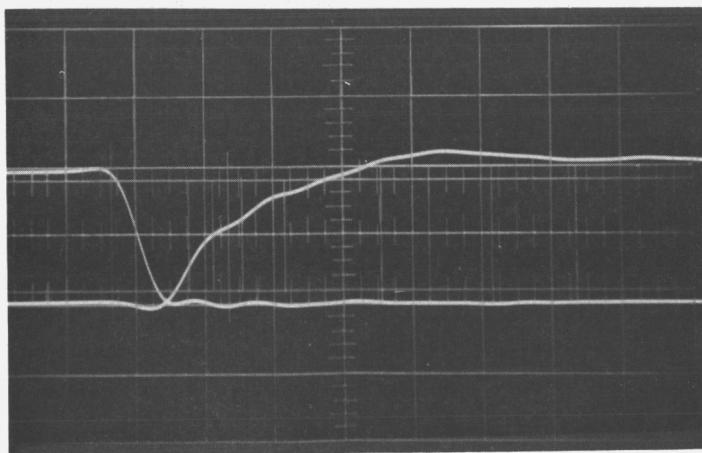Figure 79.   Switching Waveform – t_{pd0} (MF-156)
(Sheet 1 of 3)

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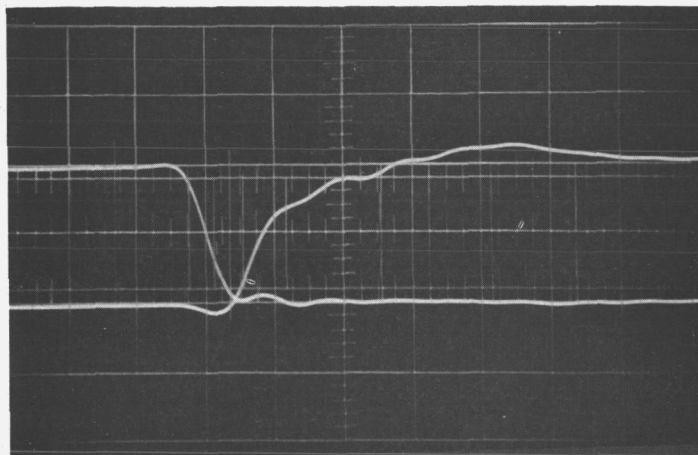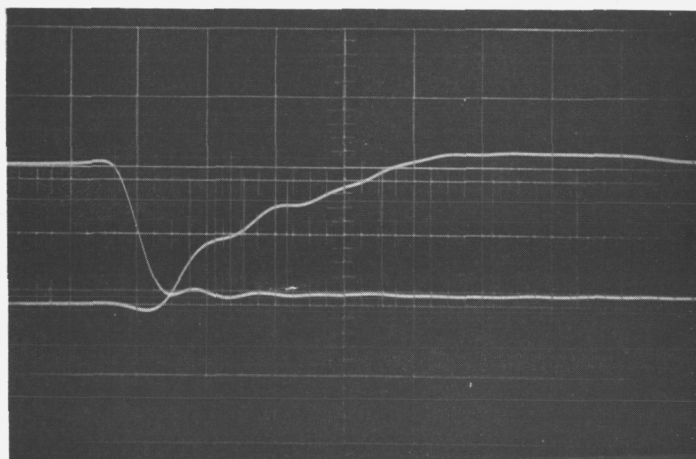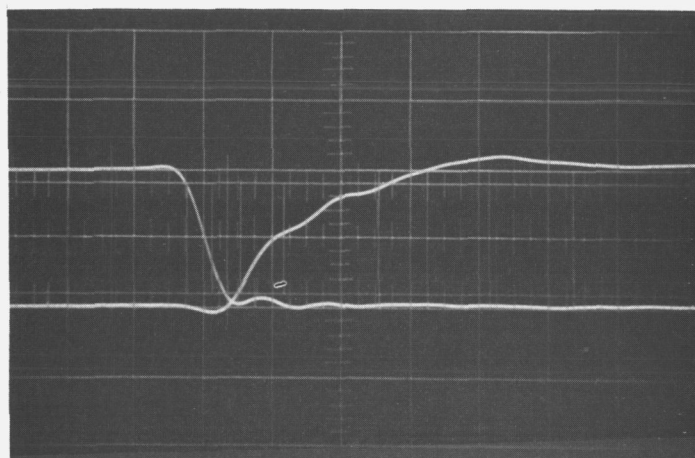(d.) NO LOAD
20 ns/DIV
25°C
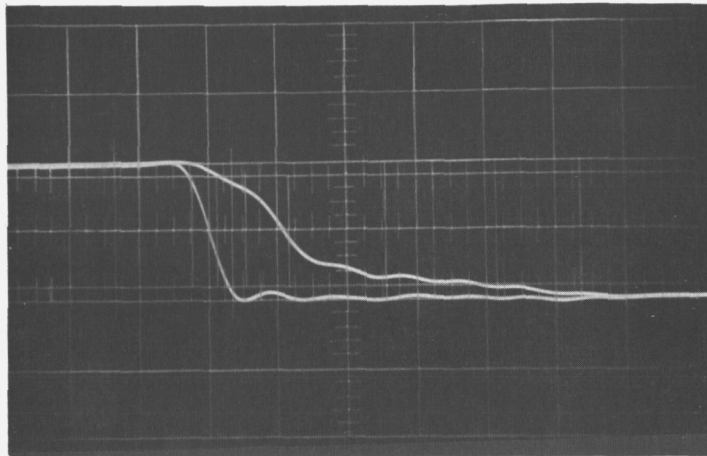
(e.) FLIP-FLOP LOAD
50 ns/DIV
25°C
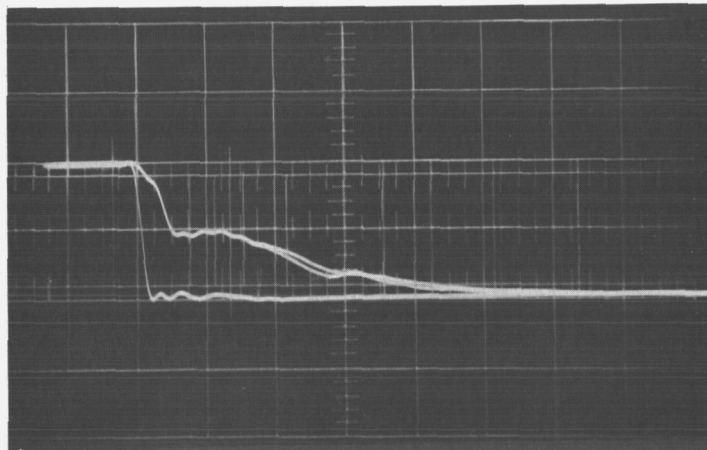
(f.) NAND LOAD
50 ns/DIV
25°C

CA16905(2-3)

**Figure 79.   Switching Waveform — t_{pd0} (MF-156)
(Sheet 2 of 3)**

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(g.) NO LOAD
20 ns/DIV
125°C

(h.) FLIP-FLOP LOAD
50 ns/DIV
125°C

(i.) NAND LOAD
50 ns/DIV
125°C

CA16905(3-3)

Figure 79. Switching Waveform — t_{pd0} (MF-156)
(Sheet 3 of 3)

(a.) NO LOAD
20 ins/DIV
-25°C
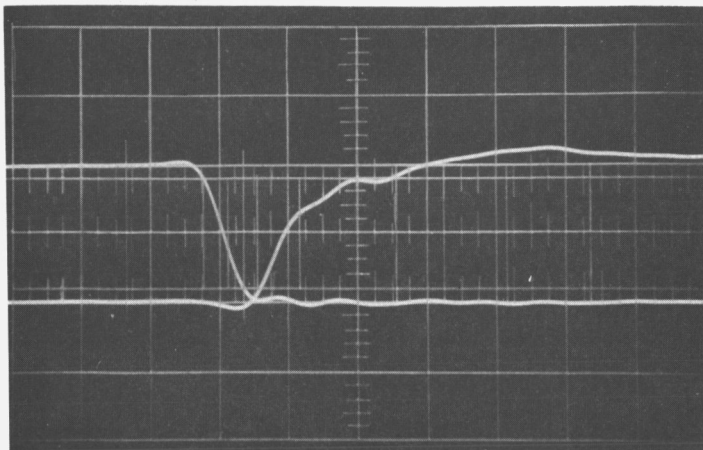
(b.) FLIP-FLOP LOAD
20 ns/DIV
-25°C

(c.) NAND LOAD
20 ns/DIV
-25°C

CA16906(1-3)

Figure 80.   Switching Waveform — t_{pd1} (MF-156)
(Sheet 1 of 3)

(d.) NO LOAD
20 ins/DIV
25°C

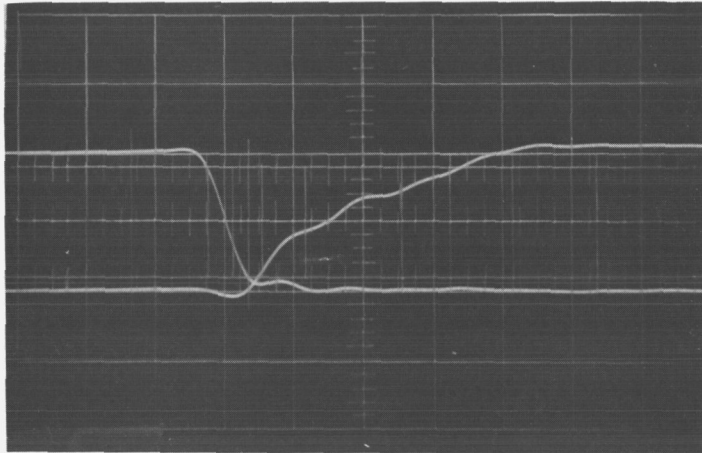(e.) FLIP-FLOP LOAD
20 ns/DIV
25°C

(f.) NAND LOAD
20 ns/DIV
25°C

CA16906(2-3)

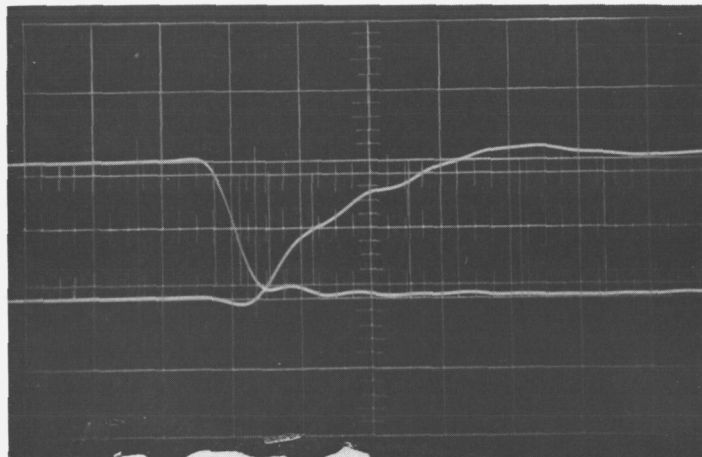**Figure 80.   Switching Waveform – t_{pd1} (MF-156)**
(Sheet 2 of 3)

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(g.) NO LOAD
20 ns /DIV
125°C
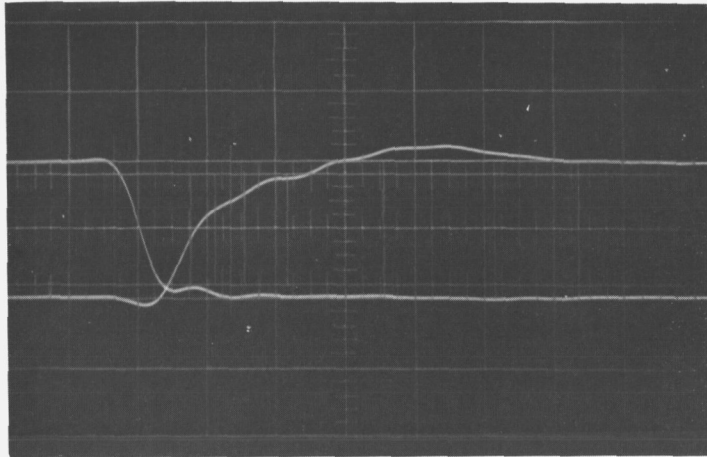
(h.) FLIP-FLOP LOAD
20 ns /DIV
125°C

(i.) NAND LOAD
20 ns /DIV
125°C

CA16906(3-3)

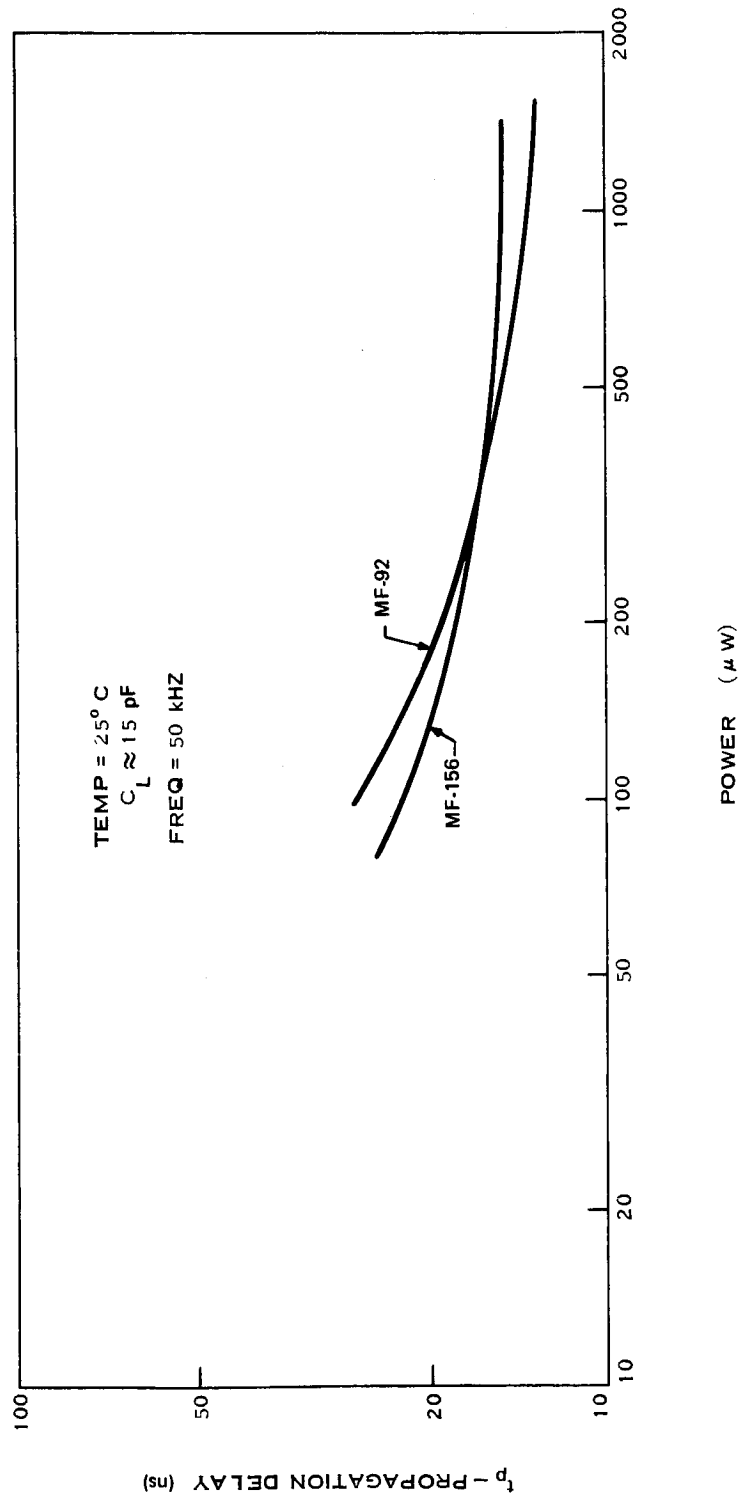**Figure 80.   Switching Waveform — t_{pd1} (MF-156)**
(Sheet 3 of 3)

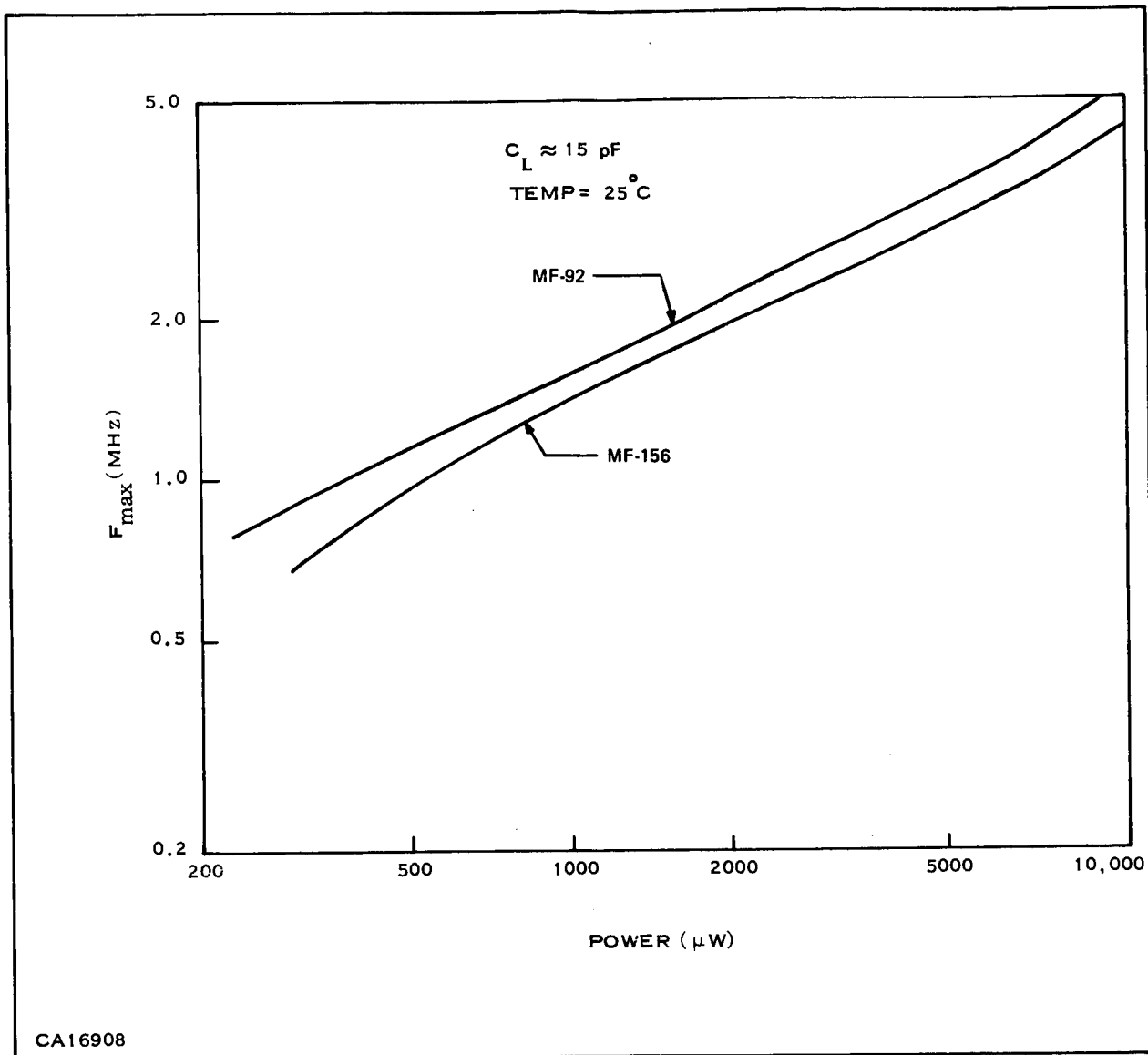Figure 81.   Propagation Delay versus Power (MF-92, MF-156)

CA16907

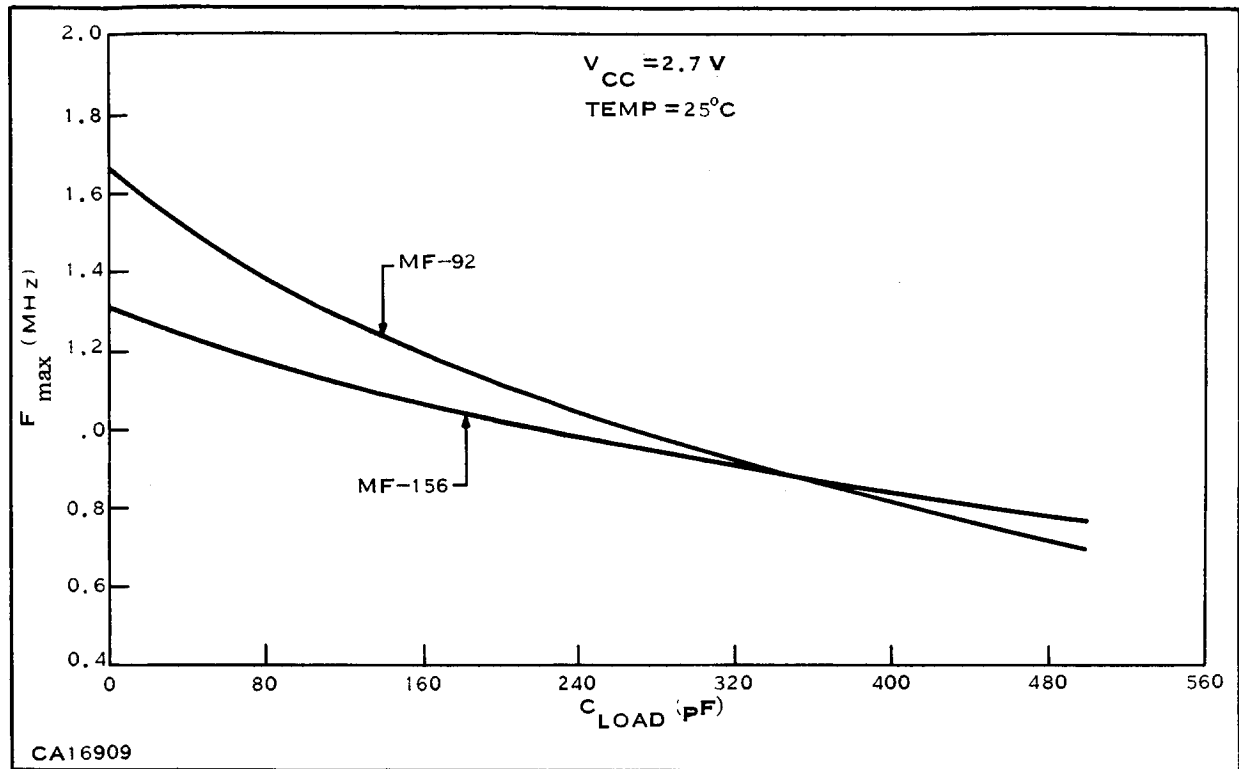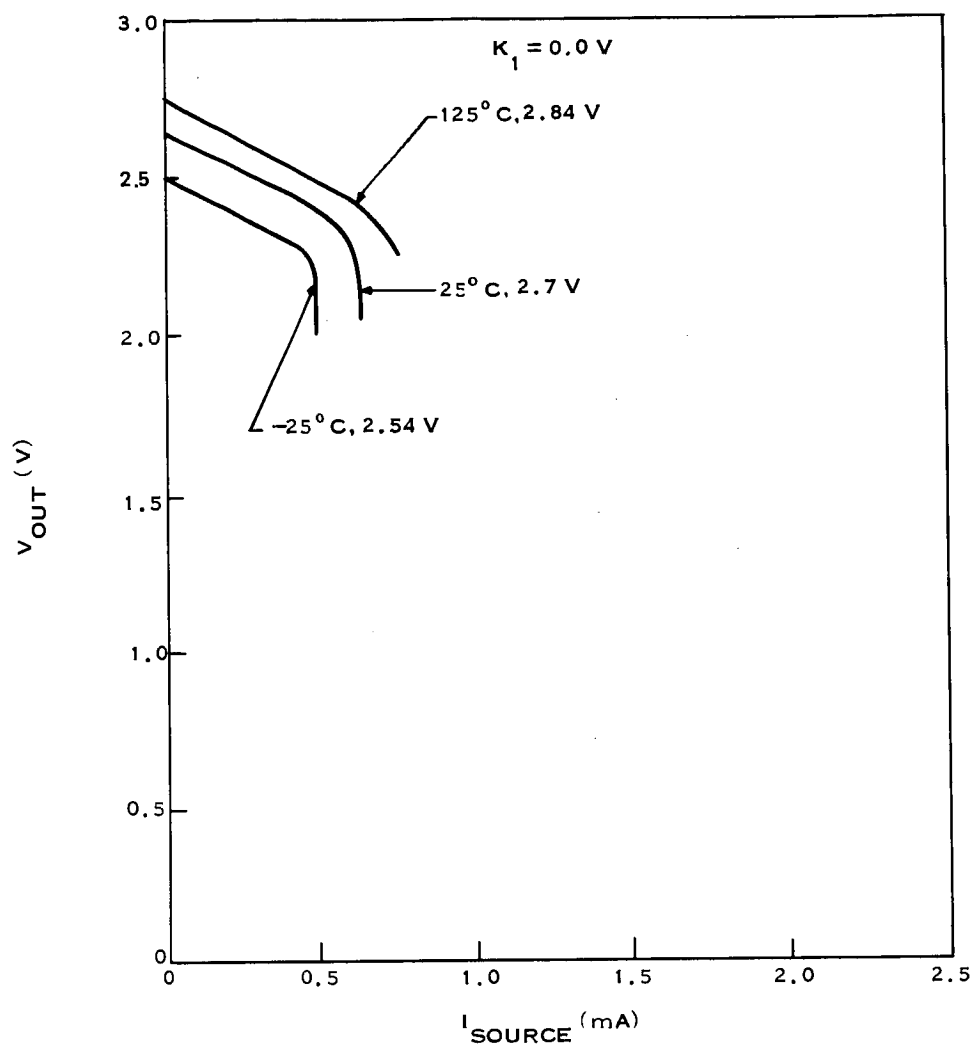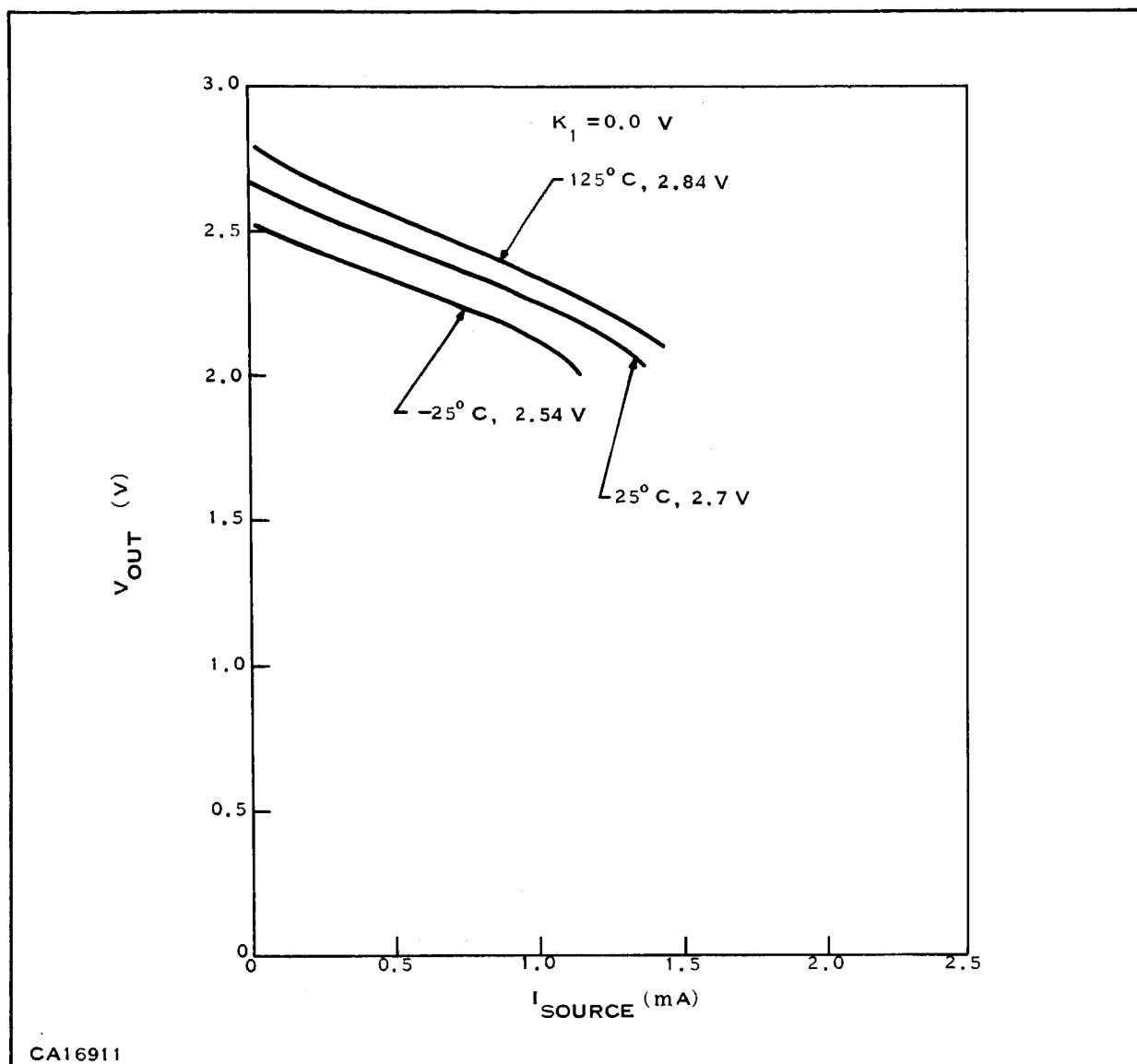Figure 82. F_{max} versus Power (MF-92, MF-156)

Figure 83. F_{max} versus C_{LOAD} (MF-92, MF-156)

Figure 84. V_{OUT} versus I_{SOURCE} (MF-92)

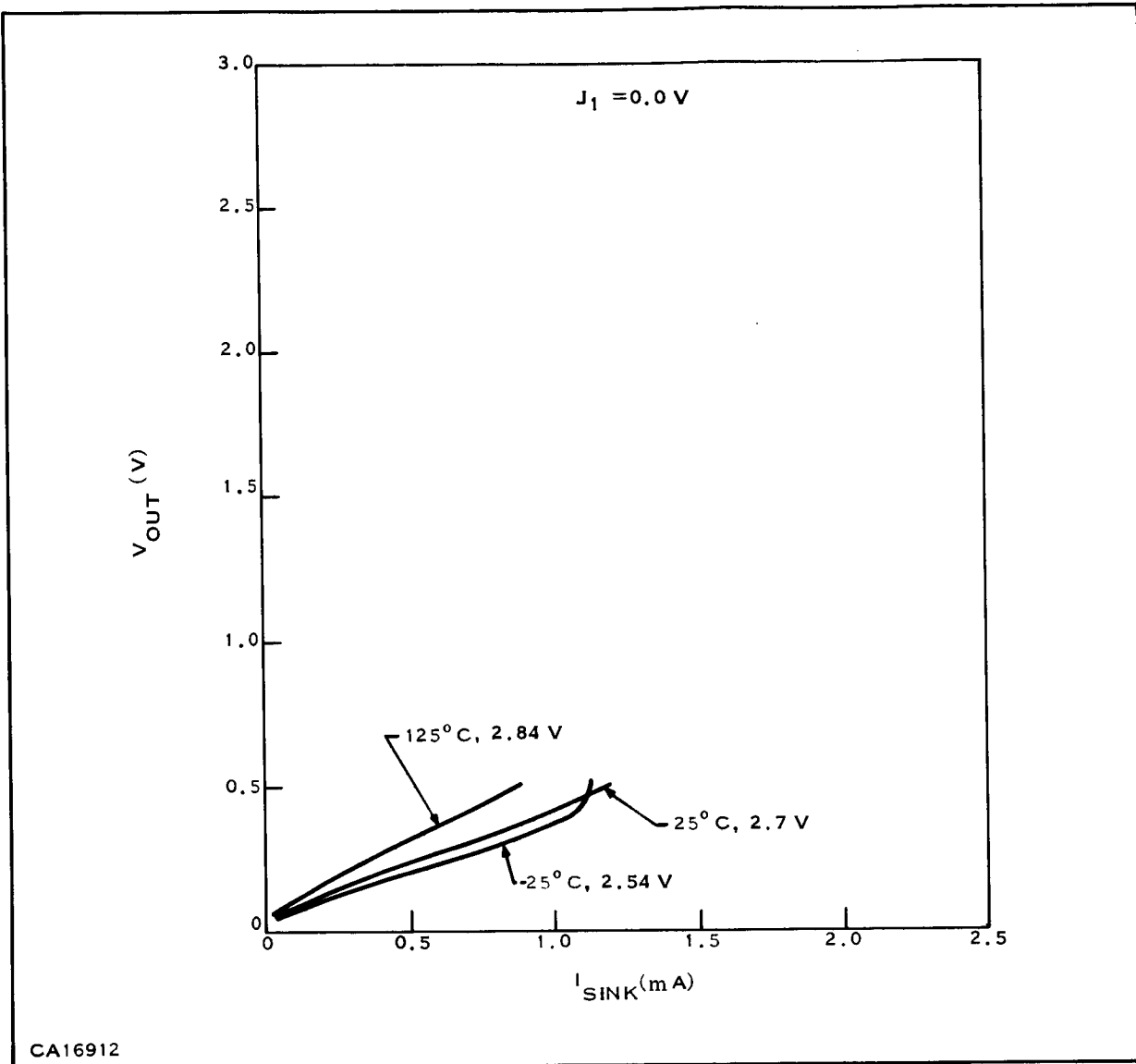**Figure 85.** V$_{OUT}$ versus I$_{SOURCE}$ (MF-156)

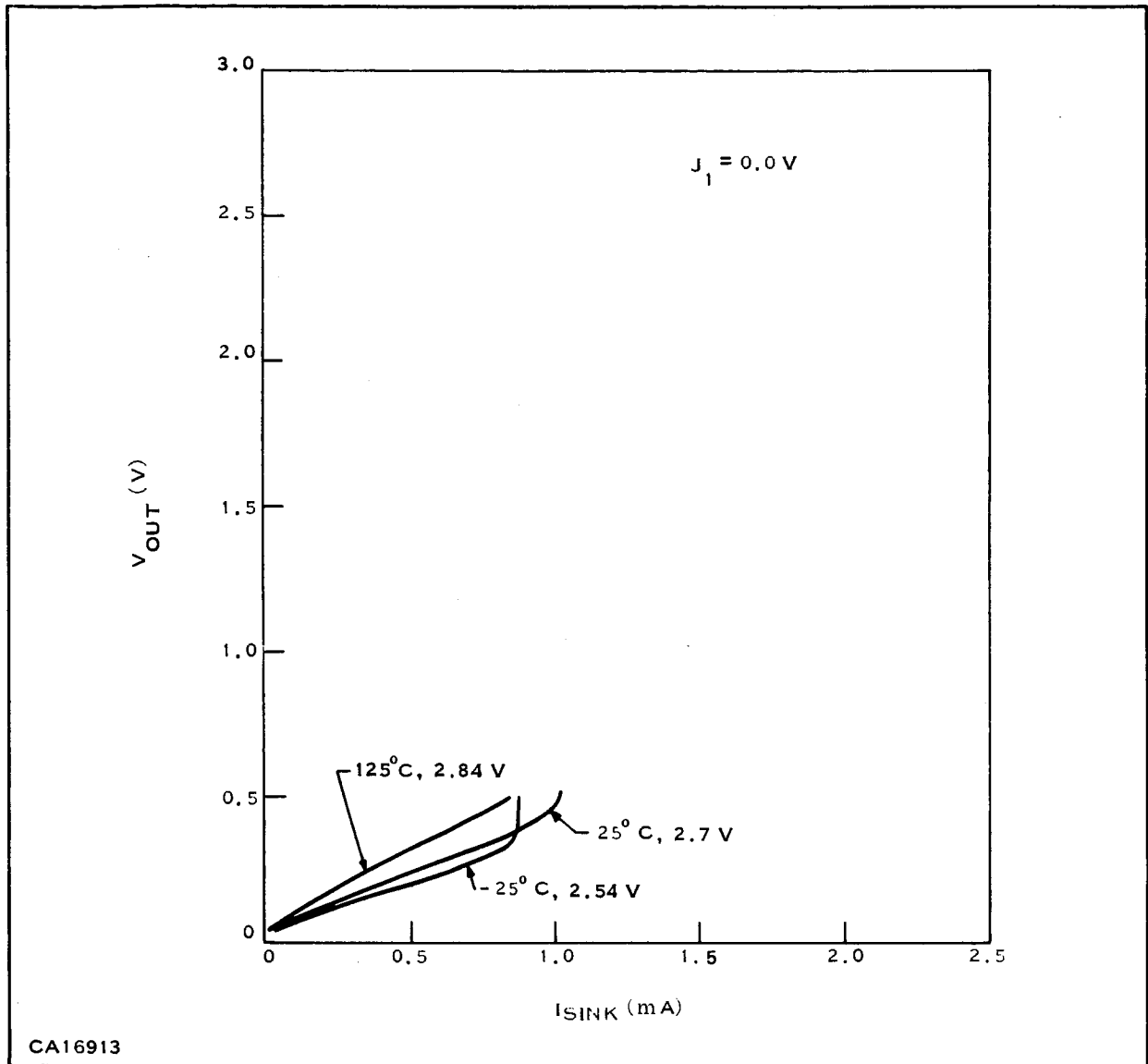Figure 86.   V$_{OUT}$ versus I$_{SINK}$ (MF-92)
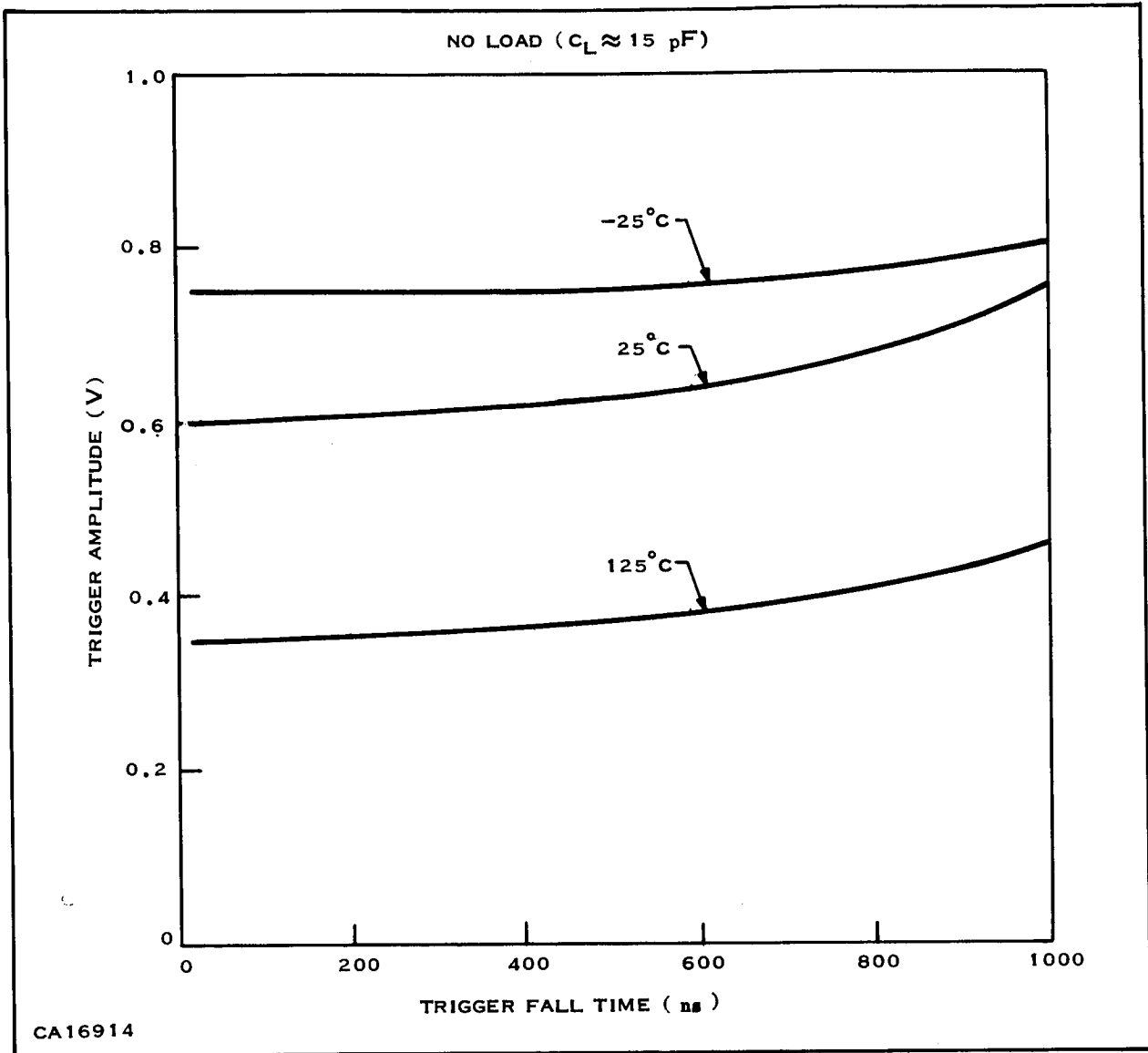
CA16912

Figure 87. V_{OUT} versus I_{SINK} (MF-156)

CA16913

Figure 88.　Trigger Sensitivity (MF-92)
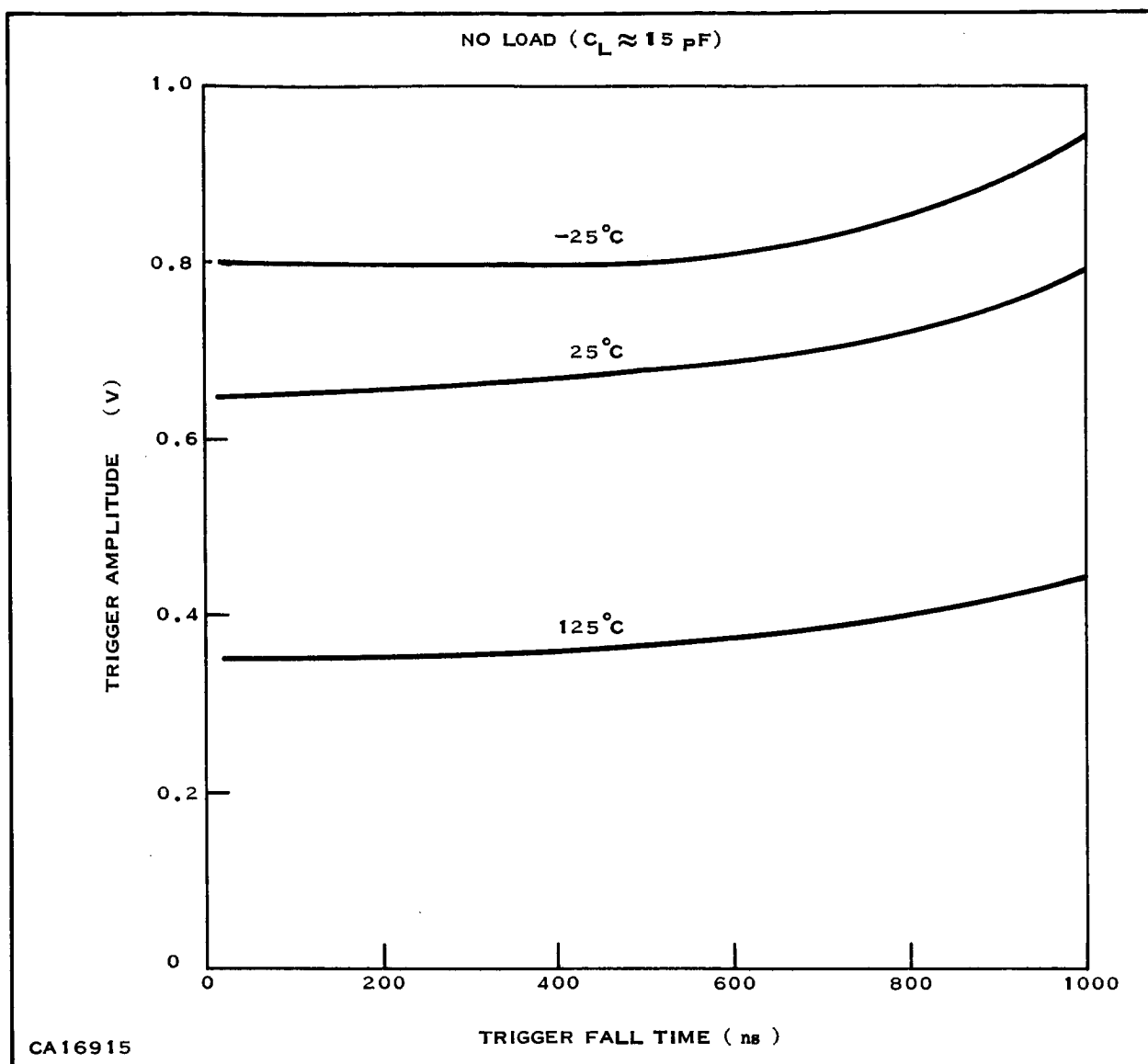
Figure 89. Trigger Sensitivity (MF-156)

NO LOAD ($C_L \approx 15$ pF)

$V_{CC} = 2.7$ V

TEMP = 25°C

(a) t_{pd0}

50 ns / DIV
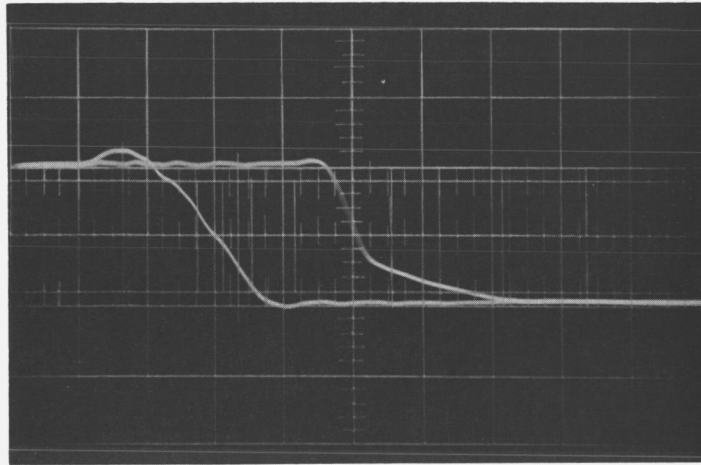
(b) t_{pd1}

50 ns / DIV

CA16916

Figure 90.   DC Set and Reset (MF-92)

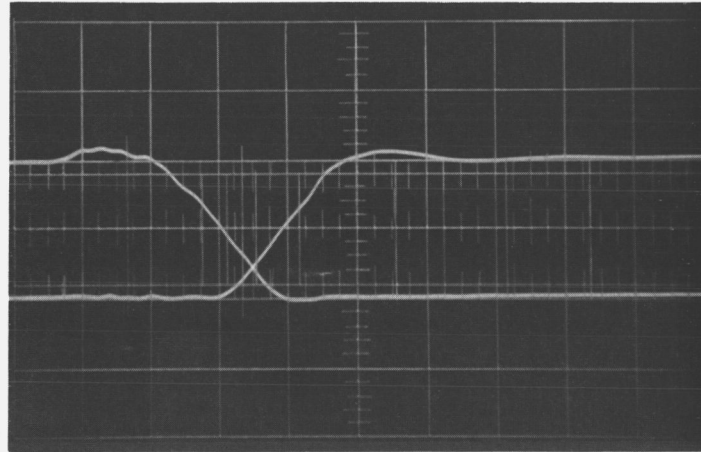NO LOAD ($C_L \approx 15$ pF)

TEMP= 25°C

V_{CC} = 2.7 V

(a). t_{pd0}

50 ns / DIV

(b). t_{pd1}
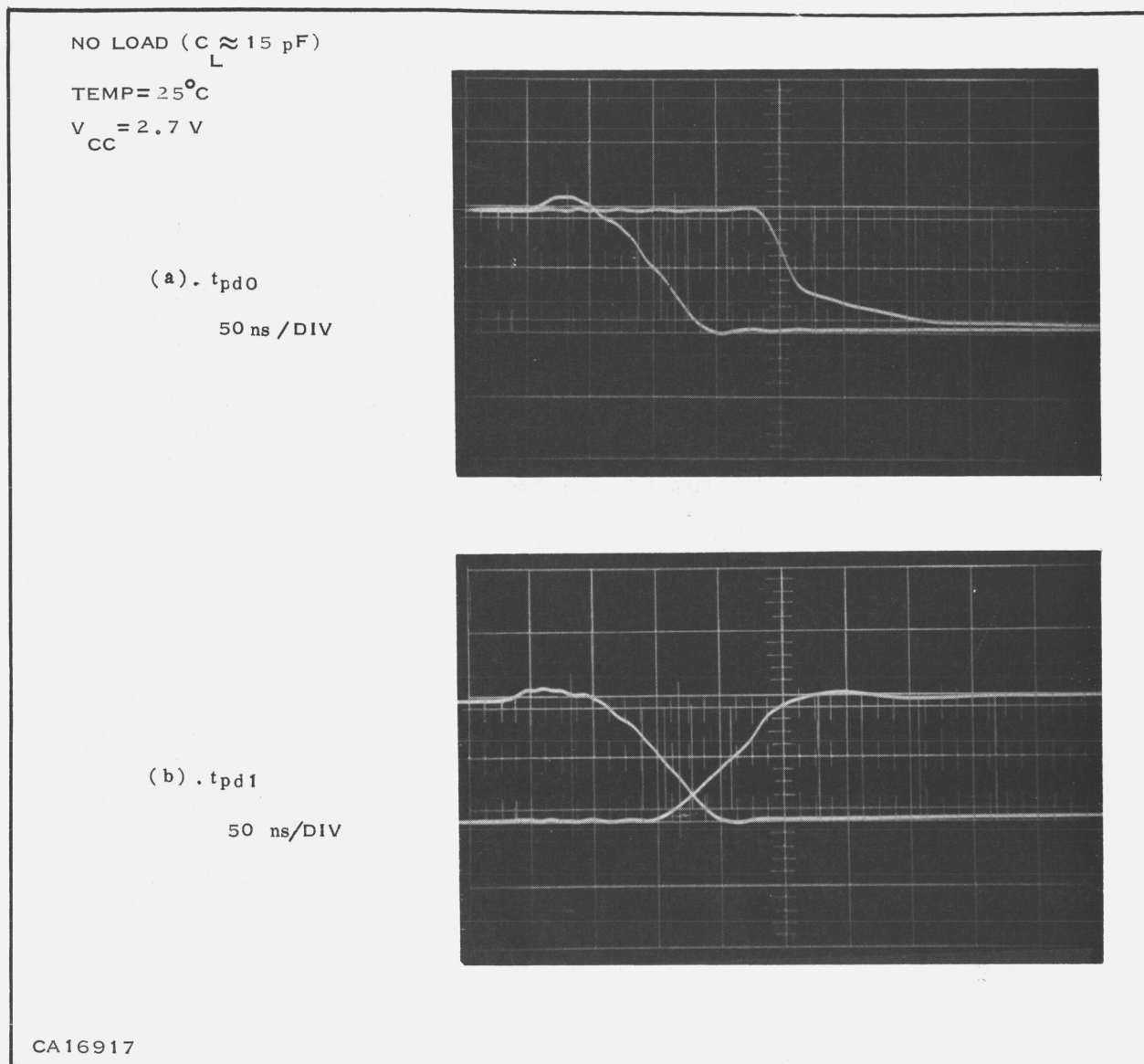
50 ns/DIV

CA16917

Figure 91.   DC Set and Reset (MF-156)
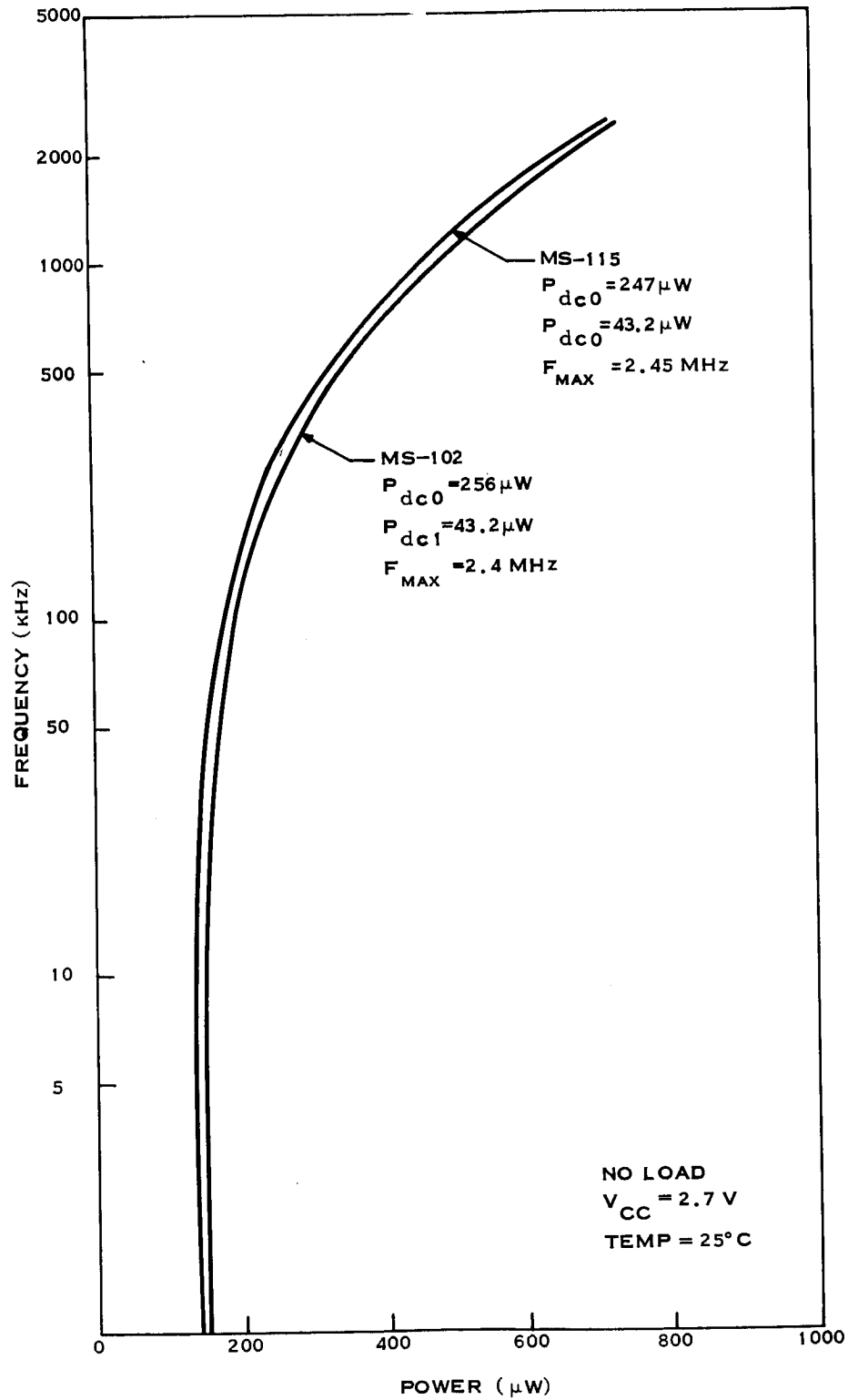
Figure 92.   Schedule B NAND Gates (Frequency versus Power)
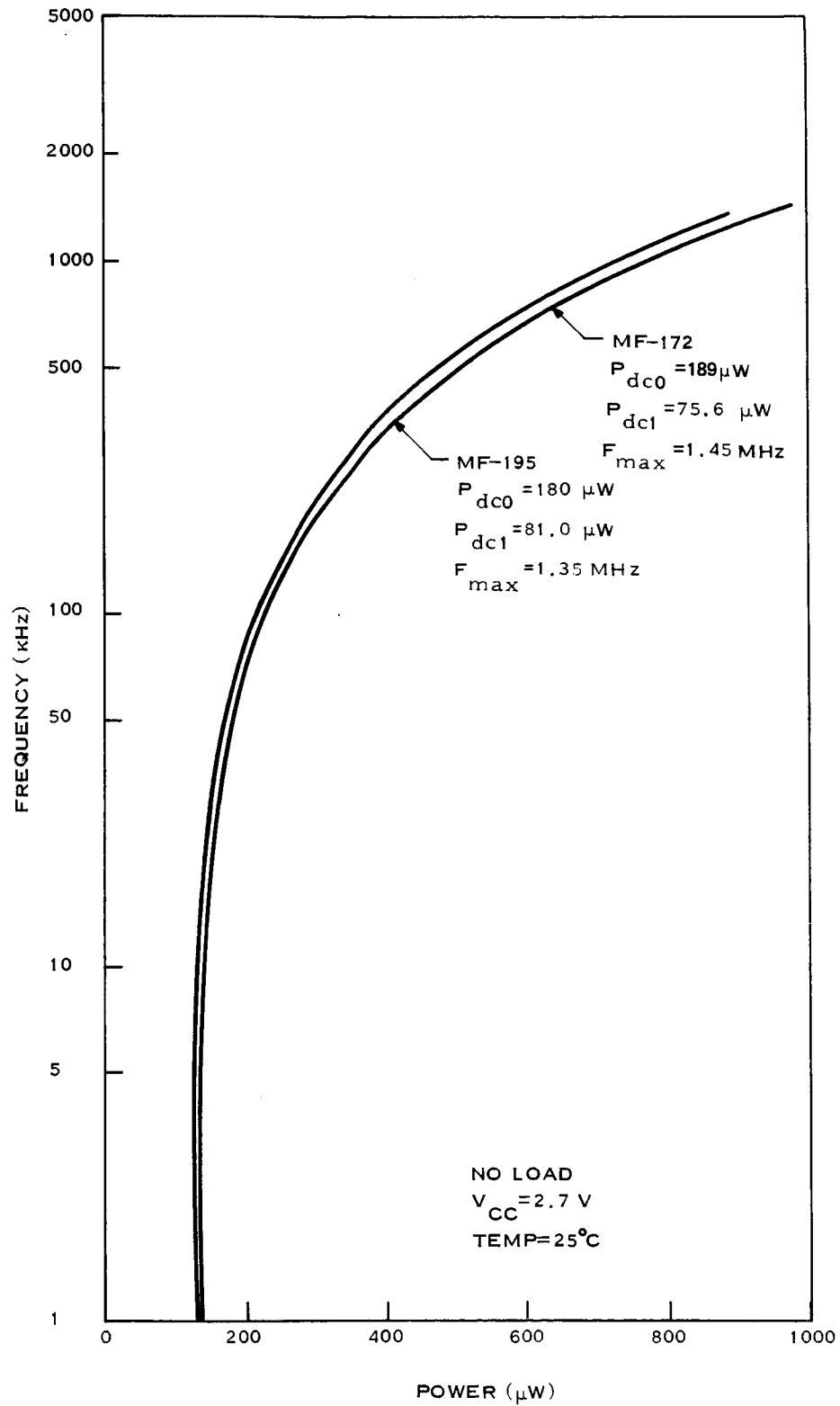
Figure 93.   Schedule B Flip-Flop (Frequency versus Power)
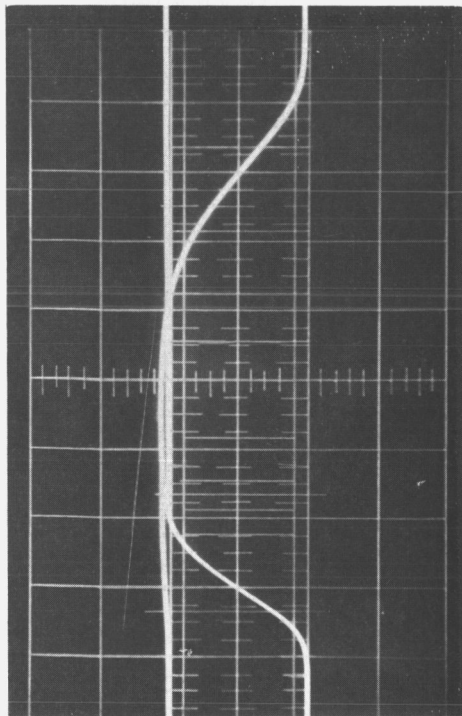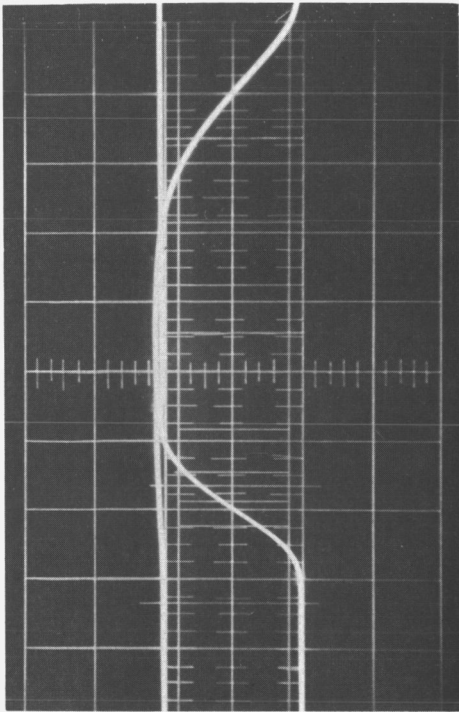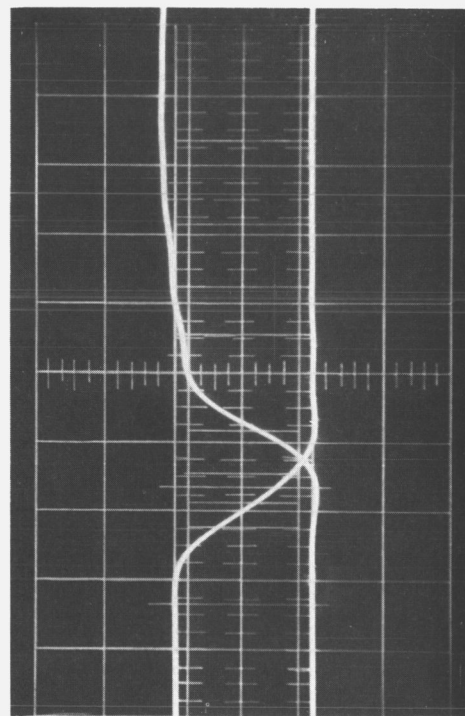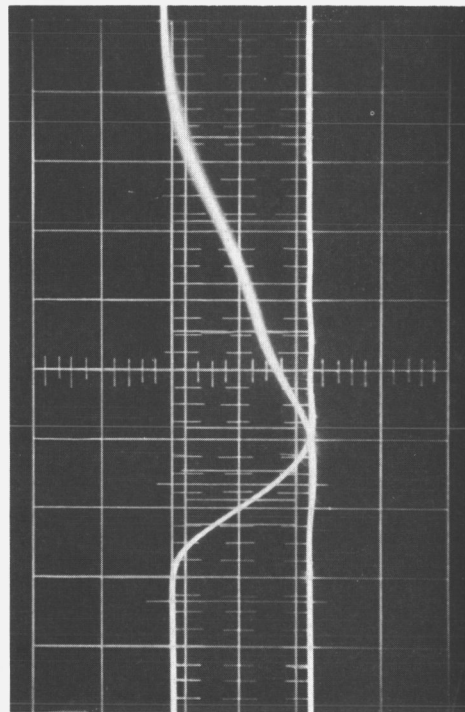
Figure 94. Switching Waveforms of Schedule B NAND Gates

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(c)   MF-192 (t_{pd0})
20 ns / DIV

(d)   MF-192 (t_{pd1})
20 ns / DIV

(a)   MF-172 (t_{pd0})
20 ns / DIV
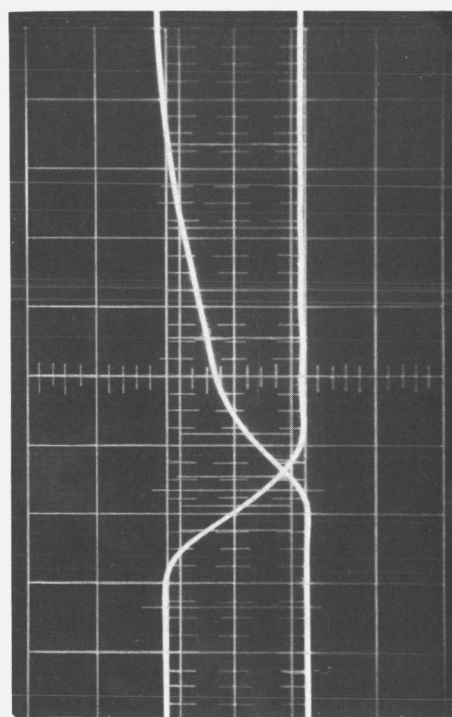
(b)   MF-172 (t_{pd1})
20 ns / DIV
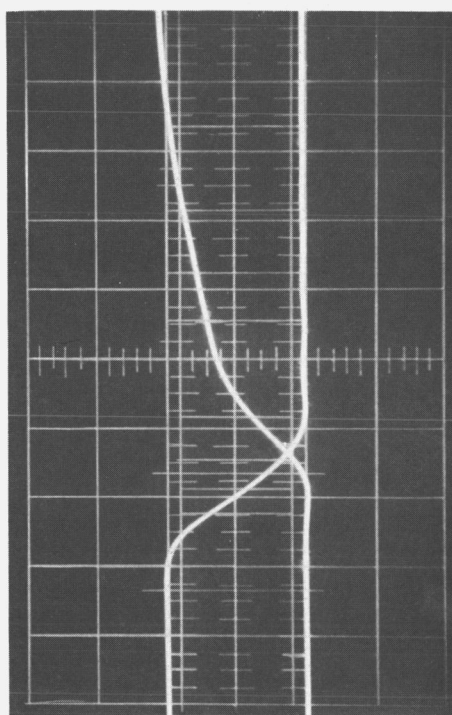
Figure 95.   Switching Waveforms of Schedule B Flip-Flops

CA16921

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SECTION III

CONCLUSIONS

All major design and performance criteria for this program were met except maximum frequency of operation for the J-K Flip-Flop. Even though this specification was not met, the results represented a 100% improvement over circuits fabricated during contract NAS1-4350, while at the same time, circuit power was reduced approximately 50 μW. The performance is summarized in Table III.

Table III. CT^{2}L Circuit Performance (NAS1-7106)

| No.	Item	NAND Gate	Flip-Flop
1.	Voltage		
	a. Nominal Value	2.7 V	2.7 V
	b. Tolerance	± 5%	± 5%
	c. Maximum V$_{CC}$ Without Damage	6.0 V	6.0 V
2.	Power Drain		
	a. "0" Worst-case Standby	300 μW	300 μW
	b. 50 kHz	200 μW	200 μW
3.	Rise Time	20 ns	20 ns
4.	Fall Time	50 ns	50 ns
5.	Propagation Delay	70 ns	20 ns
6.	Power-Speed Product	14 pJ	4 pJ
7.	Fan-out	5	5
8.	Fan-in	6	< 2-unit load
9.	Maximum Frequency	2.5 MHz	1.5 MHz
10.	DC Set or Reset Times	—	100 ns

Fabrication of high-quality micropower PNP and NPN transistors on a common substrate was demonstrated. These transistors were fabricated by a simplified process with no decrease in performance. These devices will have application in the linear monolithic area as well as in the digital.

Complementary Transistor-Transistor Logic (CT^{2}L) was shown to be adaptable to high-speed operation (2 MHz) at low power as well as an excellent standby power logic (300 μW). A power-speed product of 15 pJ was obtained for the NAND gates.

Further reduction in power and increase in switching speeds is possible with improvement in isolation techniques.

The complementary transistor fabrication and complementary logic techniques demonstrated here can be used to develop a 1.0 - V logic system.

SECTION IV

REFERENCES

1. R. H. Baker, *Maximum Efficiency Switching Circuits,* Technical Report No. 110, Lincoln Laboratory, Massachusetts Institute of Technology (March 22, 1956).

2. *Development of Micropower Microelectronic Logic Circuits,* Final Technical Documentary Report, No. 03-66-50, Contract No. NAS1-4530 (Dallas, Texas: Texas Instruments Incorporated).

3. D. K. Lynn et al., Analysis and Design of Integrated Circuits (McGraw-Hill, 1967).

APPENDIX

APPENDIX

NOTES CONCERNING OPERATION OF FLIP-FLOP

A. OPERATION AS A COUNTER

1) Connect V_{CC}, ground and clock per Figure 36. Clock should not exceed V_{CC}.

2) Output is taken from Q or $\overline{Q}$.

3) No other connections are necessary; however it is recommended that dc set and reset be returned to V_{CC} when not used.

B. OPERATION AS A SHIFT REGISTER

1) Connections same as in A.

2) Output $\overline{Q}_1$ of stage 1 goes to K_1 (or K_2) of stage 2 and so on.

3) Output Q_1 of stage 1 goes to J_1 (or J_2) of stage 2 and so on.

4) The following logic tables apply.

Tables A-I and A-II describe the individual gate functions.

Table A-I

Logic		
J_1	J_2	$J_1 J_2$
0	0	0
0	1	0
1	0	0
1	1	1

Table A-II

Logic		
K_1	K_2	$K_1 K_2$
0	0	0
0	1	0
1	0	0
1	1	1

Table A-III describes the operation when only one set of J-K inputs is used.

Table A-III

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

Table A-IV describes the operation when both sets of J-K inputs are used.

Table A-IV

t_n				t_{n+1}
J_1	J_2	K_1	K_2	Q
0	0	0	0	Q_n
0	0	0	1	Q_n
0	0	1	0	Q_n
0	0	1	1	0
0	1	0	0	Q_n
0	1	0	1	Q_n
0	1	1	0	Q_n
0	1	1	1	0
1	0	0	0	Q_n
1	0	0	1	Q_n
1	0	1	0	Q_n
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	$\overline{Q_n}$

C.   DC SET AND RESET

1)   DC set and reset is accomplished by a "0" input at the dc set and reset inputs.

2)   When not in use it is recommended that dc set and reset functions be returned to V_{CC}.